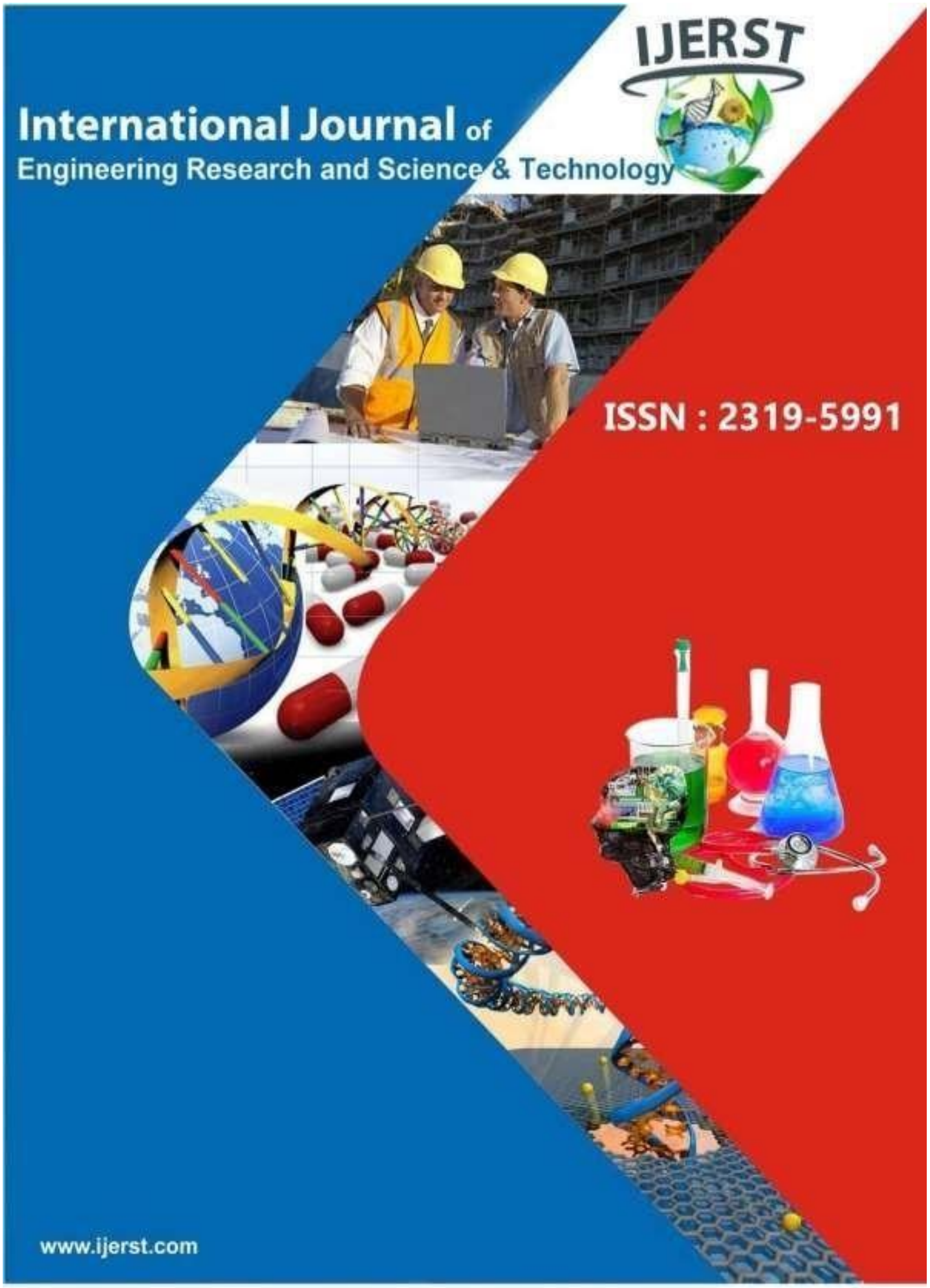

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A NOVEL CONTROL APPROACH TOAA THREE-PHASE INDUCTION MOTOR WITH OPEN-ENDED CONTROL, FED BY AN INFINITE-LEVEL INVERTER (ILI) WITH VECTOR AND SCALAR CONTROL

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ABSTRACT

This article describes the design and performance study of an open-ended, three-phase induction motor that is powered by an infinite level inverter (ILI) and has its speed controlled using both direct vector and scalar control methods. The ILI is a part of the Reduced-Device-Count (RDC) Active-Front-End (AFE) Multi-level Inverter (MLI) architecture. This inverter topology's basic components are an H-bridge and a dc-to-dc buck converter. With this architecture, there are no concerns with reverse recovery or shoot-through, allowing for high-quality power conversion. Using a resistive load, the suggested topology's performance is verified. The voltage waveform obtained has an output THD of 1.2%. Furthermore, there has been a high level of dc-source voltage consumption with this configuration. Because just one high-frequency switch is run at a time per phase while the other switches are operated at power frequency, ILI significantly lowers switching and conduction losses. The inverter has a 98% total efficiency. Using scalar and direct vector control approaches, the speed control performance of the ILI architecture with a three-phase open-ended induction motor has been further confirmed. Verification of simulation study results is done by experimentation.

INDEX TERMS: three-phase infinite level inverter, scalar and direct vector control, multi-level inverters, active front-end, decreased device count

I. INTRODUCTION

In power electronic applications like electric drives, hybrid and electric cars, uninterruptible power supplies, HVDC power transmission, renewable energy integration, Flexible AC Transmission Systems (FACTS), and static VAR compensators, dc-to-ac inverters are becoming increasingly important. The inverters may be generically categorized as two-level or square wave inverters, quasi-square wave inverters, two-level PWM inverters, and multilevel inverters (MLI) based on how the output voltage waveform develops and is structured.

One of the main issues with traditional or two-level inverters is that they need more powerful semiconductor components. A large number of devices must be linked in series or parallel strings in order to achieve the necessary voltage and current capacity. Consequently, these inverters produce output waveforms with poor power quality and increased conduction loss. Therefore, MLI may be selected as a superior option in order to get over the aforementioned problems [1]. In the last thirty years, MLIs [2][7] have garnered significant interest from the scientific and industrial communities because to their superior power conversion capabilities, including increased efficiency, control, and power quality when compared to all other traditional inverters. Producing a greater number of voltage levels with less distortion is the fundamental idea behind MLI. Multiple low-rated power semiconductor switches and different dc low voltage levels carry out the power conversion. Every level is identified as the section of the voltage waveform where the voltage magnitude stays constant for a certain amount of time, resulting in the formation of a voltage waveform resembling a staircase. The output voltage waveform's power quality grows as the number of voltage levels does. Due to MLIs' practical technology for implementing regulated speed drives and maintaining power quality in high-power applications, their demand in current industrial applications has skyrocketed.

The basic topologies of MLIs may be divided into three groups: i. Neutral Point Clamped (NPC) or Diode Clamped [10], ii. Flying capacitor (FC) [11], and iii. Cascaded H-Bridge (CHB) [2], [8], [9]. People refer to them as classical topologies. The first two of these basic topologies must have a single DC source, whereas the third topology need numerous DC sources. However, additional passive components and semiconductor devices are needed to implement such topologies. As a result, the system becomes heavy and complicated. Modular structure, sometimes known as modularity, is one of the multilevel structure's most desired characteristics. Because of its flexibility, the CHB topology outperforms the others in terms of output voltage, power level, and dependability. NPC and FC topologies are practically practicable only up to five layers; at this point, their structure and control implementation grow more complex, and the number of devices for various ratings also rises significantly. However, since all of CHB's devices have the same power rating, it is the best option for higher levels. However, since too many power semiconductor devices must coordinate with one another and because more dc sources are needed to provide a bigger number of levels, the control implementation is more complicated [9]. Numerous new application-focused MLI topological advancements have been documented in a variety of literatures, in addition to the classical topologies.

Basically, they are developed from hybrids of traditional topologies. None of the topological innovations of the new generation, meanwhile, can be seen to be wholly beneficial. The majority of them are made for certain uses. Application-oriented topologies have often prioritized boosting output voltage levels and power quality while decreasing switching device counts, passive component counts, and overall cost. In [12][19], a few application-oriented techniques are covered. Fault-tolerant topology is another important advancement in MLIs. A fault-tolerant architecture has been presented by Chen et al. [20] to get an uncompromised multilevel voltage waveform in the event that there is a partial failure in the power circuit. These topologies use several switching states' redundancy and control signal modification to maintain the output voltage waveform. Glinka made another significant addition to MLI topologies. The "Modular Multilevel Converter (MMC)" is a novel single DC source-based multilevel architecture that was introduced by [21].

This MMC stands out for its scalability and versatility. Compared to a CHB inverter, this architecture is simpler. In theory, it may theoretically achieve any desired voltage level with fewer harmonic problems, lower converter component ratings, and increased efficiency. Medium- and high-power energy conversion systems, industrial applications such as FACTS, medium-voltage variable-speed drives, HVDC transmission systems, and medium-to-high voltage dc-to-dc converter applications have all shown interest in the suggested topologies. A review study on MMC was provided by Suman Debnath et al. [22]. It is emphasized with a broad summary of the fundamentals of operation, control difficulties, cutting-edge control techniques, and application difficulties. The majority of MLIs are created by arranging several Sub Module (SM) configurations that may link to one another to build both traditional and contemporary MLIs. A broad overview of MLIs based on primary submodules was given by Vijeh et al. [23]. Reducing the device count (RDC) in MLI topologies has been the focus of research efforts over the last several decades. In addition to lowering total loss, cost, size, and complexity, MLIs may increase system efficiency and reliability by using fewer passive components and semiconductor switches. Numerous unique RDC-MLI topologies have been documented in various literatures [24]–[34]. Each of the aforementioned topologies has advantages and disadvantages depending on the needs of the application. A thorough analysis of a few newly created RDC-MLI topologies, which are better suited for various applications such machine drives, renewable energy systems, and FACTs, was provided by Bana et al. [35]. Both independent and grid-tied apps may employ these topologies. Three major categories may be used to categorize RDC-MLI topologies. The H-bridge type MLIs that are reduced are reduced switch symmetric (RSS-MLI) [36], [37], and reduced switch asymmetric (RSA-MLI) [38]. While reduced switch modified MLI (RSM-MLI) [39]–[41] topologies lack an H-bridge, the configurations discussed above often consist of an

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RDC-MLI linked with an H-bridge. Numerous unique topologies have been seen in a variety of literatures in recent years.

Active Front End (AFE)-RDC-MLI topology is the overall structure of these currently in use topologies. The dc-to-dc converter being used determines which of these current MLI topologies are used. These topologies consist of a synchronized H-bridge after an AFE converter (dc-to-dc converter). The primary function of the H-bridge architecture is polarity generation (inverter), while the primary function of the AFE converter is voltage level generation. Numerous literatures [42]–[53] address alternative AFE–RDC–MLI topologies.

The three-phase AFE-RDC-MLI topology for an open-ended three-phase induction motor drive application is designed and its performance analyzed in this study. Using a high switching frequency, a dc-to-dc buck converter is used in this suggested architecture to generate various voltage levels. The AFE converter's switching frequency determines the output voltage levels that are produced. An increase in switching frequency corresponds to a corresponding rise in output voltage levels. Higher voltage levels cause the output voltage waveform to become smooth and sinusoidal. The levels produced in the output voltage waveform become endless if the AFE converter's switching frequency is pushed to almost infinity. As a result, the output voltage waveform's power quality is improved. Consequently, the infinite level inverter (ILI) topology is the name given to the suggested topology.

Both an open-ended three-phase induction machine and a resistive load have been used to verify the suggested topology's performance. The outcomes derived from the simulation research are confirmed using experimental means. TABLE 1 provides a quick discussion of MLI taxonomy. The suggested MLI topology offers a number of benefits.

1) Only one high-frequency switch per phase is in operation.

2) Power frequency is used while operating an H-bridge inverter circuit.

3) Because there are inductors positioned between the voltage source and the inverters, this design is not vulnerable to shoot through threats.

4) Electrolytic capacitors, which are more affordable and smaller than ac capacitors, may be used as the output filtering capacitors in AFE converters.

5) Complex algorithms may be implemented using this architecture.

6) The researchers' sophisticated control techniques for dc-to-dc converters may be directly

implemented into the system. The AFE converter can be controlled more freely since it works at high switching frequency ranges. 7) The system performs dynamically well. Thus, even in the presence of significant fluctuations in the supply voltage or load currents, the output voltage maintains its dynamic stability. 8) The architecture based on dc-to-dc converters is very compatible with the implementation of closed-loop control systems. The following are this article's principal conclusions.

• An induction motor powered by a three-phase infinite level inverter is designed, analyzed, and operated.

• Very high-quality voltage and current waveforms with little THD were seen in this design when tested with a resistive load.

• SPWM control validates that the dc-voltage needed to provide a fixed ac-voltage output is much less than that of other comparable topologies.

• This inverter has also been used to implement the third harmonic injection modulation technique, where it was discovered that there is still room for improvement in the dc-source usage.

• Because just one switch is operated at a high frequency per phase, it has also been discovered that the inverter's efficiency is higher. In typical inverters, every switch is operated at a high frequency.

• Using this structure, induction motor control has also been accomplished both scalar and vector. With this design, it has been discovered that both controls show improved dynamic performance. Furthermore, it has been discovered that an induction motor drive performs better when the ILI is used.

• The voltage delivered across the motor's terminals in a normal inverter circuit would be an absolute discrete number, such as Vdc, −Vdc, Vdc/2, −Vdc/2, etc. As a result, there would be a significant instantaneous error voltage between the applied voltage and the intended sinusoidal voltage. This erroneous voltage causes torque ripples in the motor, which reduces the motor's efficiency.

• The applied voltage in the buck converter-based architecture described in this study is nearly exactly sinusoid, meaning that there is very little applied voltage error.

As a consequence, the motor experiences very little torque pulsations, which improves motor performance. To enable the three buck converters to be coupled to the same voltage source, open ended windings are employed. These days, Wide Band Gap (WBG) devices, such as silicon carbide (SiC) and gallium nitride (GaN), are replacing theoretically better and high frequency operable counterparts, the old silicon (Si) power semiconductor devices, in the power and electronic sectors and their application domains [54]. High-frequency switches are taking the place of typical Si technology with the introduction of WBG materials. Further performance and efficiency gains will occur if WBG semiconductor devices are employed in lieu of the Si semiconductor devices used in ILI architecture. As a result, the system can operate at higher frequencies and becomes more compact. The structure of this document is as follows..

2. THREE-PHASE INFINITE LEVEL INVERTER TOPOLOGY

2.1 THREE-PHASE INFINITE LEVEL INVERTER TOPOLOGY

An H-bridge is placed after a buck converter in an infinite level inverter's fundamental construction. The only goal of the suggested architecture is to reduce the number of power semiconductor and passive element count while maintaining power conversion power quality. In the meanwhile, it lowers the circuit's size, control complexity, and switching and conduction losses. A three-phase ILI topology is obtained by combining three separate ILI circuits, as seen in Fig. 1. Each buck circuit in the suggested topology has one high-frequency controlled switch, and each H-bridge has four low-frequency operated switches; this means that each phase has one inductor and one capacitor. Compared to other comparable inverter topologies and typical two-level topologies, this architecture has a low voltage stress across the switches and a high dc-source voltage utilization. This circuit's other features include reduced reverse recovery loss, body diode conduction loss in semiconductor switches, and the lack of a shoot-through problem.

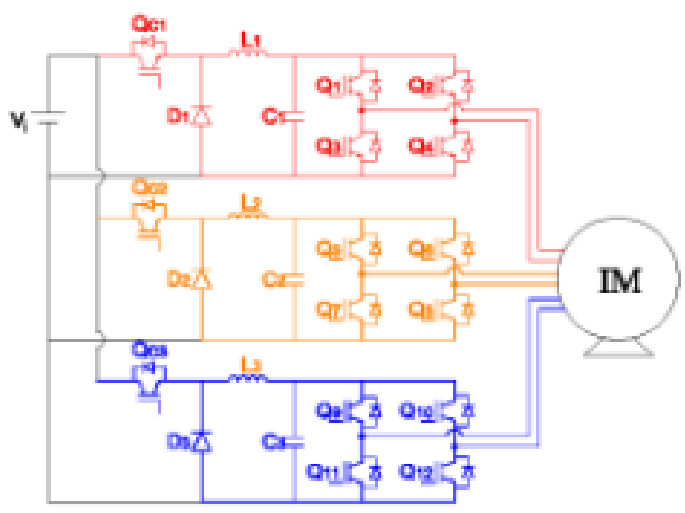

FIGURE 2.1. Three phase Infinite Level Inverter topology.

The basic building block of the suggested topology is an H-bridge, which is followed by a buck converter (AFE converter). With this architecture, there is one inductor and one capacitor per phase because each buck circuit has one high-frequency driven switch and each H-bridge has four low-frequency operated switches.

2.2 PRINCIPLE OF OPERATION

Each level in an MLI is the area of the voltage waveform where the voltage magnitude stays constant for a certain amount of time. There is never a moment in the ILI when the voltage stays steady; it fluctuates constantly. The voltage waveform becomes a pure sine wave if the period of time during which the voltage stays constant goes to zero. By altering the buck circuit's duty cycle in a completely

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rectified sinusoidal fashion, the AFE converter produces a fully rectified infinite level voltage waveform. The AFE converter's switching frequency determines the quality of the output voltage. The ILI's SPWM control logic is shown in Fig. 2. Given the buck

capacitor, the number of voltage levels created across it is given by

$$V_{Level} = \frac{f_c}{f_m}$$

MODES OF OPERATION

There are four modes of operation for this inverter. They are discussed with the help of Fig. 3 Mode-1: During the period δT , the switch Qc1 is turned ON, and the inductor current starts rising. The diode is reverse biased. The output capacitor is charged exponentially. Mode-2: During the period (1 − δ) T , switch Qc1 is turned OFF, and the parallel diode starts conducting. The current through the inductor falls, and it freewheels through the diode. In modes 1&2, Q1 and Q4 are conducting, so that a positive voltage is obtained across the load. Hence it generates the output voltage as +ViM |sin(ωt)| across the load side. Mode-3: is same as mode-1, except for the fact that Q2 and Q3 are switched ON. Mode-4: is same as mode-2, except for the fact that Q2 and Q3 are switched ON. Hence it generates the output voltage as −ViM |sin(ωt)| across the load side. The output voltage developed across the inverter load terminal is Vo = ViMsin(ωt); 0 6 ωt 6 2π.

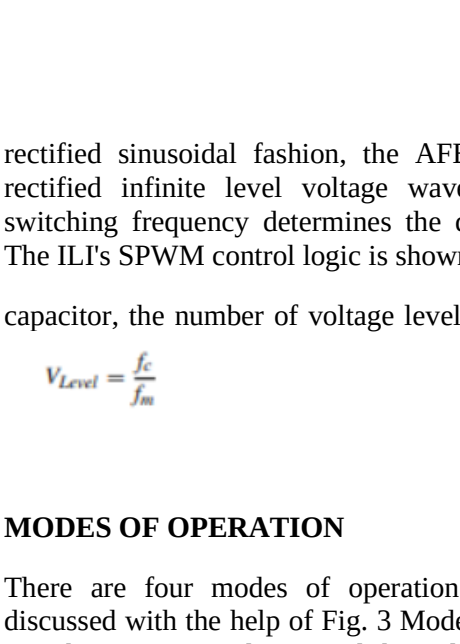


FIGURE 3. Mode of operations. (a) Mode-1, (b) Mode-2, (c) Mode-3, (d) Mode-4.

3. SCALAR AND VECTOR CONTROL OF ILI FED INDUCTION MOTOR

This section addresses the use of several control systems, including scalar (V/f) and direct vector control, to regulate the speed of an open-ended three-phase induction motor. High dynamic performance in controlling the induction motor speed is possible with the suggested ILI architecture. 1. SCALAR (V/F) MANAGEMENT MODE Due to its ease of use and simplicity, the V/f control approach is a popular way to regulate the speed of an induction machine. Fig. 8 displays a block schematic of the implementation logic for scalar control. Here, the stator voltages and frequency may be adjusted proportionately to manage the air-gap flux of the induction machine at the required value. As so, the machine operates at any speed while maintaining its torque/ampere capacity. In the meanwhile, under steady-state conditions, the machine speed may be precisely maintained at any specified value. However, the torque capability is limited at low speeds because to the dominating voltage drop across the stator winding resistance.

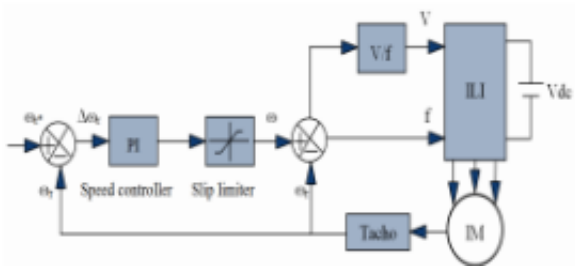


FIGURE 3. Scalar control of ILI fed induction motor implementation logic.

3.1 DIRECT VECTOR CONTROL METHOD

Fig. 9 displays the direct vector control system's block diagram. Here, utilizing is used to compute the field angle.

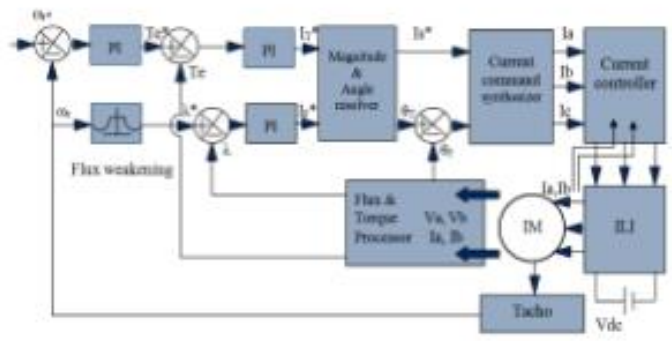
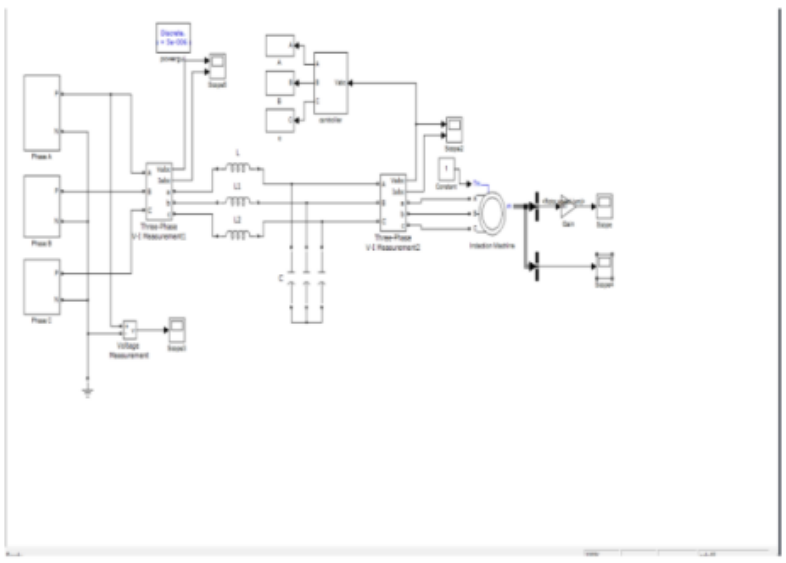


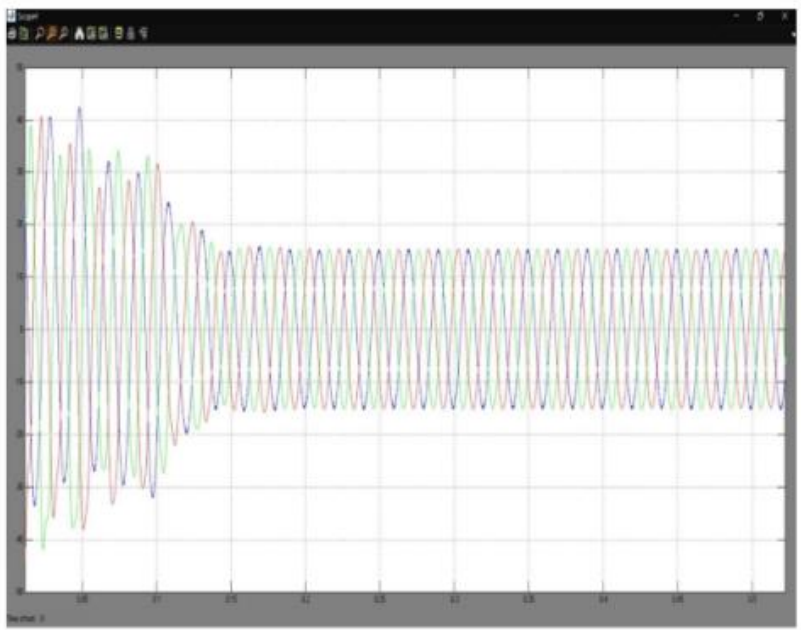
FIGURE 3.1 Direct vector control of ILI fed induction motor

4. MATLAB & SIMULATION RESULTS

4.1 SIMULATION CIRCUIT:



4.2 OUTPUT WAVEFORM ACROSS THE LOAD:



4.3 OUTPUT WAVEFORM ACROSS THE BUCK CAPACITOR:

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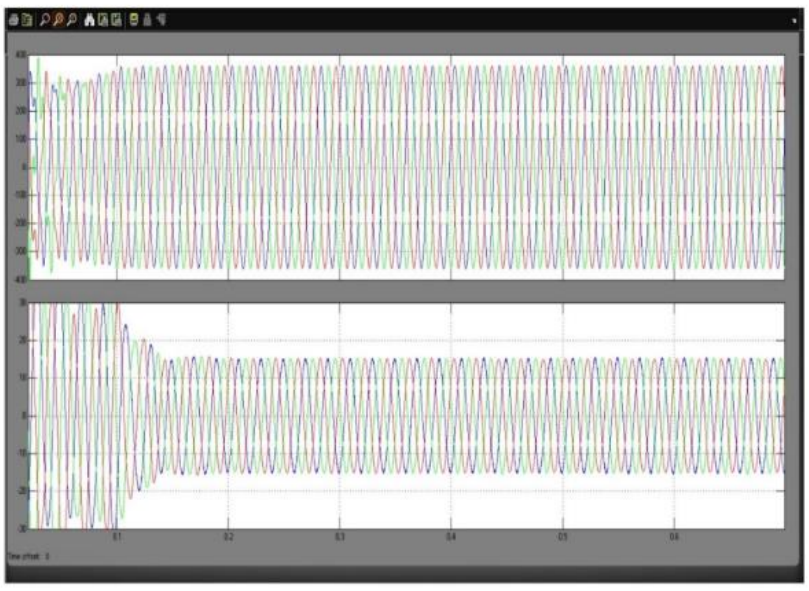
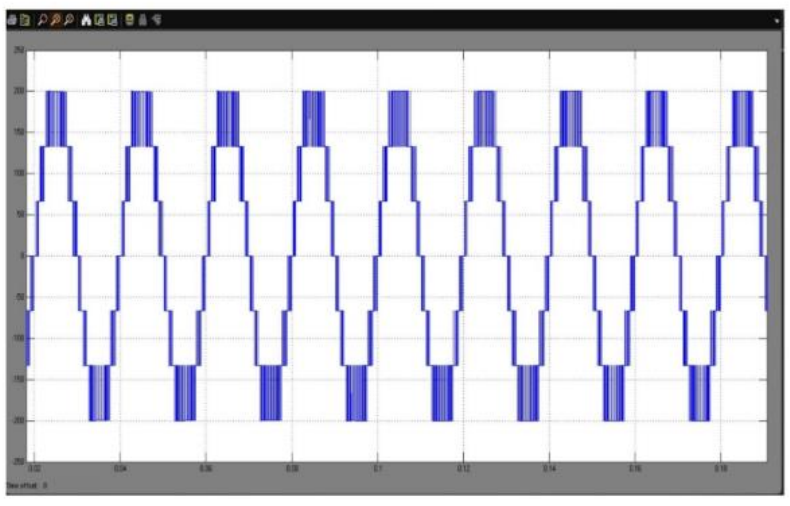
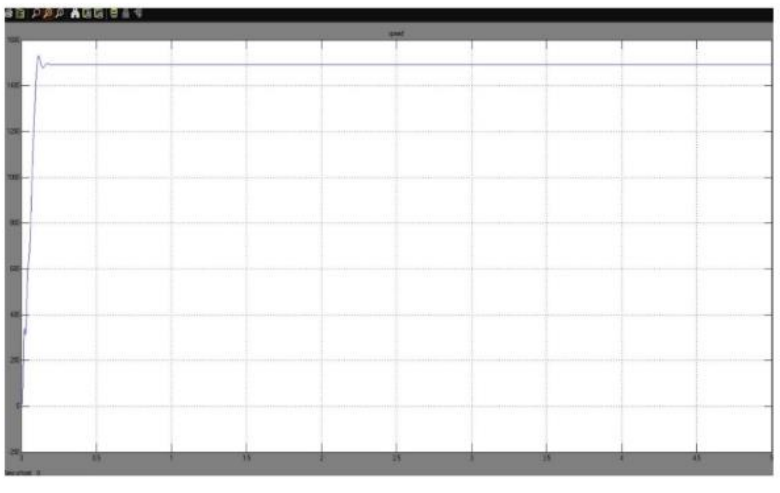


4.4 OUTPUT WAVEFORM ACROSS THE 3 LEVEL H-BRIDGE INVERTER:



4.5 SPEED WAVEFORM:



5.CONCLUSION

This study has addressed the design and performance analysis of an infinite level inverter powered induction motor. It has been discovered that ILI improves an induction motor drive's performance. When evaluated with a resistive load, the AFERDC-MLI topology's ILI was found to have exceptionally high-quality voltage and current waveforms in terms of THD. The inverter architecture discussed in this work has a THD of only 1.2%, compared to tens of percentages in standard inverter topologies. Furthermore, it has been shown that the dc-voltage needed to generate a fixed ac-voltage output is far less than that needed by other topologies of a similar nature, improving the dc-source usage with this topology.

A traditional inverter operating in sine PWM mode has a dc voltage need of 677V, but the new inverter only needs a 338V dc voltage requirement. This inverter has also been used to test the third harmonic injection modulation technique, and it was discovered that additional improvements in dc-source usage are possible. Since just one switch per phase is run at a high frequency, it has also been discovered that the inverter's efficiency is improved. In typical inverters, every switch is operated at a high frequency. Using this structure, scalar and vector control of induction motors have also been implemented. It has been discovered that this architecture provides superior dynamic performance. By using several reference speeds to accelerate and decelerate the machine, this has been verified. Given the very low harmonic content of the current, the torque pulsations the motor experiences would be minimal. In this instance, there is no need for the de-rating often associated with induction motors powered by traditional inverters. The drive system has a longer lifespan and is more reliable since there is less risk of damage to the inverter due to the lack of shoot-through threat.

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