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A study of Enhancement in Power Consumption and Energy Efficiency Using Bandwidth Scheduling

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ABSTRACT

The transfer of big data in various applications across high-performance networks (HPNs) in anationalorinternationalscopeconsumesasignificantamountof energy onadailybasis.However, most existing bandwidth scheduling algorithms only consider traditional objectivessuch as data transfer time minimization, and very limited efforts have been devoted to energyefficiency in HPNs. In this paper, we consider two widely adopted power models, i.e. power-down and speed-scaling, and formulate two instant bandwidth scheduling problems to minimizeenergy consumption under data transfer deadline and reliability constraints.The model showsthat today the access network dominates the Internet's power consumption and, as access speedsgrow, the core network routers will dominate power consumption. The power consumption ofdata centers and content distribution networks is dominated by the power consumption of datastorage for material that is infrequently downloaded and by the transport of the data for materialthat is frequently downloaded. Based on the model several strategies to improve the energyefficiency of the Internet are presented.The performance superiority of the proposed solutions isillustrated by extensive resultsbased on both simulated and real-lifenetworks in comparisonwithexistingmethods.

KEYWORDS: High-performancenet works,bandwid the scheduling,energy efficiency.

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1.INTRODUCTION

TheInternethasbecomeanintegralcomponentoftheeconomiesofalldevelopedanddevelopingnations. Thevirtualcycleofimprovementsintelecommunicationssupportingeconomic growth,which,in turn,supports growth in telecommunicationsinfrastructure hasserved many nations very well. However, this cycle cannot continue without end because alltelecommunications networks require resources to function, particularly (electrical) power, tooperate. The larger the network becomes (in both capacity and physical size) the more electricalpower it consumes. Today the information and telecommunications sector is responsible forapproximately5percentofthetotalelectricalpowerconsumptionindevelopednationaleconomies [1]. The Internet's infrastructure consumes approximately 1 percent of a developednation's total electricity consumption in these countries [2–5]. This percentage will grow ashigher-speed national broadband access networks are rolled out over the coming years. The rateof growth of the Internet, in terms of both uptake and capacity increase, means that actuallyreducingits total power consumption is unlikely to be a realistic goal. The network is growingtoofast.Amorepracticalgoalistoimprovethe‒energyefficiency‖oftheInternet.Byenergy efficiency we mean the amount of data that could be conveyed from end to end per quantum ofenergy consumed by the network. This measure of energy efficiency is simply the reciprocal ofthe energy per bitof data transported and/or processed. Note thatalthough we identify thoseparts of the Internet that dominate its power consumption (i.e., watts or watts/user), we discussmethods for improving energy efficiency (i.e., reducing Joules per bit). The relationship betweenthese two quantities is power consumption (watts) is equal to energy efficiency (Joules per bit)multiplied by the traffic volume (bits per second). We adopt this approach because the Internet isa complex engineering structure, and any attempt to improve the overall energy efficiency is bestfocused on those parts that consume the most power. Therefore, a key step in this process isidentifyingthoseparts.

2. CHOOSINGTHERIGHTPROCESSTECHNOLOGY

Migrating to a smaller process technology node has always provided higher integration, lowerpower,andgreaterperformancethanthepreviousnode,and28nmisnoexception.The28-nm

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process delivers clear performance benefits, but to realize the full potential of these benefits, theproper ―flavor‖of the 28-nm process must be selected. Altera chose TSMC's 28-nm High-Performance (28HP) HKMG process and leveraged its seventeen-year-long relationship withTSMC to optimize the process forlow power on Stratix V FPGAs. This 28HP process alsoallowsStratixVFPGAstoprovide28-Gbpspower-efficienttransceiversforultra-highbandwidth applications. The exceptional performance of the 28HP process is driven not only bythe introduction of HKMG, but also by the second generation of advanced strain technology,including embedded silicon germanium (SiGe) in source-drain regions of transistors for fastercircuit designs. Altera produces tensile strain in NMOS transistors through a cap layer, andcompressive strain for PMOS transistors through embedded SiGe in the source and drain (seeFigure 1). These strained silicon techniquesincrease electron and holemobility by up to 30%and the resulting transistor performance by up to 40%. Because better performance at the samelevel of leakage is achieved with strained silicon, part of this performance gain is traded forreduced leakage, leading to a superior process that has faster performance and lower leakagecompared to other 28-nm process options without strained silicon. No other 28-nm process flavorhas this potent combination of HKMG and advanced strain available for maximum performancecharacteristicsofdevicesmanufacturedonthatprocess.

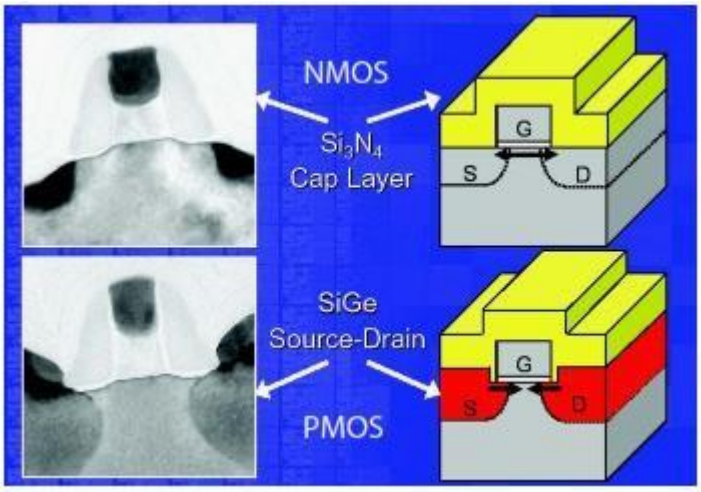

Figure1.StrainedSiliconTechniqueson28HPProcessEnableHigherPerformanceTransistor s

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Altera took full advantage of the various 28HP process capabilities to reduce power and increaseperformance. Table 1 summarizes the various process innovations and techniques leveraged byAltera on the 28HP process toreduce static power by 25% versus the standard 28HP processfromTSMC.

Table1.ProcessTechniqueson28HPtoReducePowerandIncreasePerformance

Process Techniques on 28HP	Lower Power	Higher Performance
Custom low-leakage transistors *(1)*	✔	
Custom low bulk leakage (Ibulk) *(1)*	✔	
Longer channel length transistors	✔	
HKMG	✔	✔
SiGe strain (PMOS)		✔
Si3N4 strain (NMOS)		✔
Lower capacitance	✔	✔
Lower voltage (0.85 V)	✔	

In addition, Altera leveraged the lower voltage offered by the 28HP process to significantlyreduce power without impacting performance. Figure 2 shows the static power and dynamicpowersavingsachievedbyStratixVFPGAsona0.85-Vsupply(onmostdevices)comparedtoa 1.0-V supply. Static power is proportional to Vcc3, and by reducing voltage from 1.0 V to 0.85V, the static power is reduced by 39%. On the other hand, dynamic power is proportional toVcc2,anda voltage reductionfrom1.0Vto0.85V leadstoa28%powerreduction.

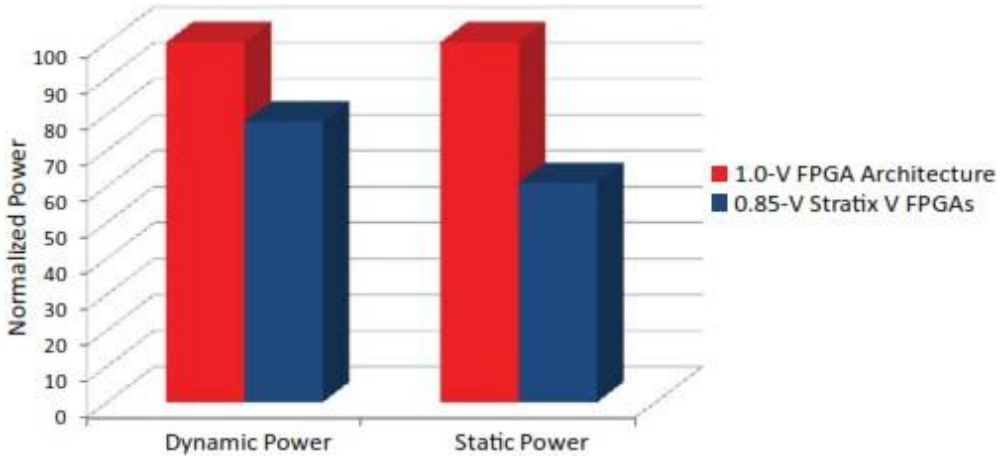

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Figure2.Static and Dynamic Power Comparison for Same Architectureon Same Process at 0.85Vand1.0V

3.FPGA ARCHITECTUR ALINNOVATIONS

Altera has been leading the industry in introducing architectural innovations, enabling designersto lower power and increase bandwidth in their system designs. The most recent four generationsof Stratix series FPGAs show a clear trend of lower power and higher bandwidth with everyprocess node shrink. As shown in Figure 3, Stratix V FPGAs enable designers to achieve 5Xhigher bandwidth at 80% lower total power compared to Stratix II FPGAs.Stratix V FPGAs arebased on the high-performance architecture of Stratix IV FPGAs and deliver key architecturalinnovationstoenabledesignerstoachievehigherbandwidthandlowerpowerthroughanun precedented level of system integration and ultimate flexibility. These innovations include theintroduction of the Embedded HardCopyBlocks, 28G transceivers, and partial reconfiguration.Stratix V FPGAs continue to leverage the highly successful Programmable Power TechnologyusedinStratixIIIandStratixIVFPGAs.

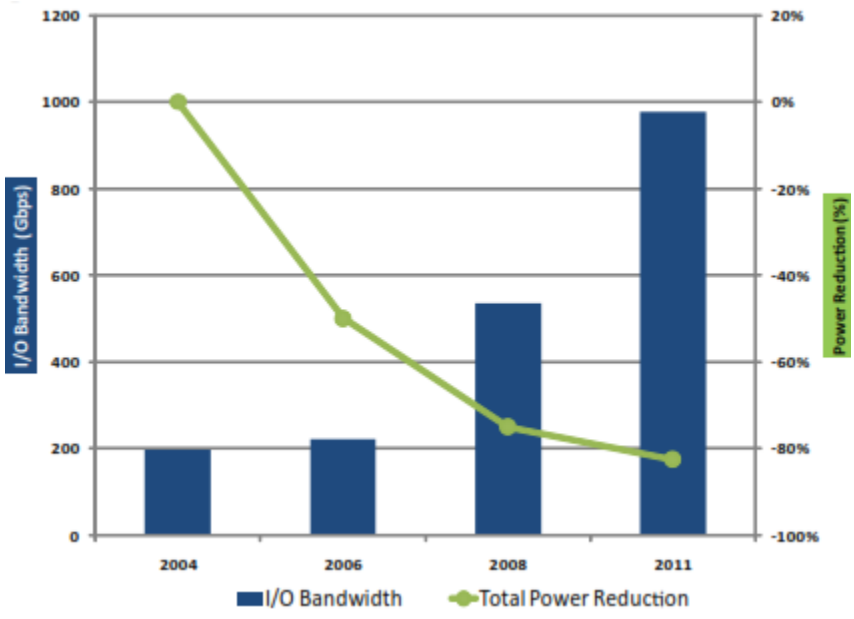

Figure3.Powerand BandwidthTrendsinStratixSeriesFPGAs

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4. HIGH-BANDWIDTH,POWER-EFFICIENT TRANSCEIVERS

Another key innovation introduced by Altera on 28-nm is the power-efficient 28-Gbps high-speed serial transceivers shown in Figure 4. These 28-Gbps transceivers are designed for chip-to-chip and chip-to-module applications and targeted to address the trend in the wireline market tomove to28-Gbpsinopticalmoduleinterfaces.

Optical modules are used in communication and computer systems to convert electrical signalsreceivedtooptical signals and then todrive them to optical fiberchannels. Similarly, theyconvert the optical signals to electrical signals and drive them to electrical copper channels. Theevolution of the optical module focuses on increasing data rates, lowering power, and reducingform factor by removing components off the module. These challenges get pushed off to siliconandsystemdesign.

Today, 100 GigabitEthernet(100GbE) networks are implemented with electrical interfacesutilizing a 10-lane by 10- or 11-Gbps signaling rate. Given the characteristics of the opticalsolutionsbeingdevelopedbyvariousindustrybodies,thecurrentdriveisforanarrowerelectrical interface with four lanes in each direction. To address this trend, 28-Gbps signalingprotocols for chip-to-chip and chip-to-module applications are being created, an example beingCommon Electrical I/O 28 Gbps (CEI-28G). This protocol will enable smaller and more cost-effective optical modules (such as CFP2) with lower power dissipation for multiple 100-Gbpsapplicationsonasingleline card.

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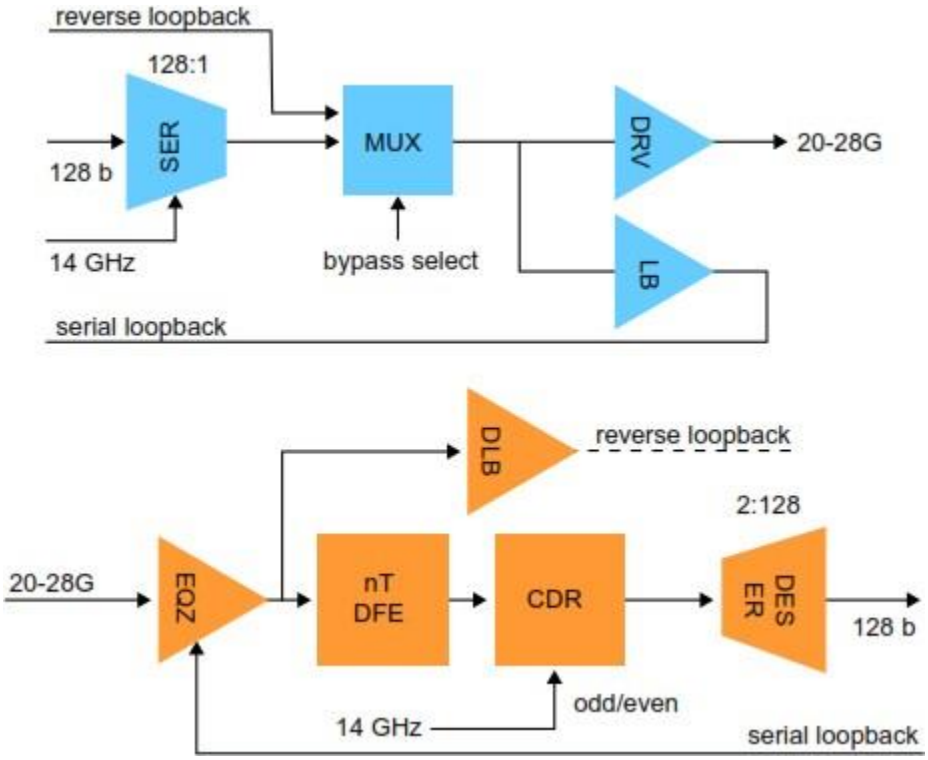

Figure4.28-GbpsTxand RxArchitecturein StratixVFPGAs

With28-Gbpstransceivers,designerscanreachhigherbandwidthandlowerpowersimultaneously.

Figure 5 shows two implementations of 100GbE interfaces to opticalmodules.In the first implementation, 10 channels, each running at 11.3 Gbps, interface with an 100G(CFP) optical module and consume 1.58 W. In the second implementation, four channels, eachrunning at28-Gbps, interface with nextgeneration 100G (CFP2) optical modules, consuminghalfthepowerat0.8W.

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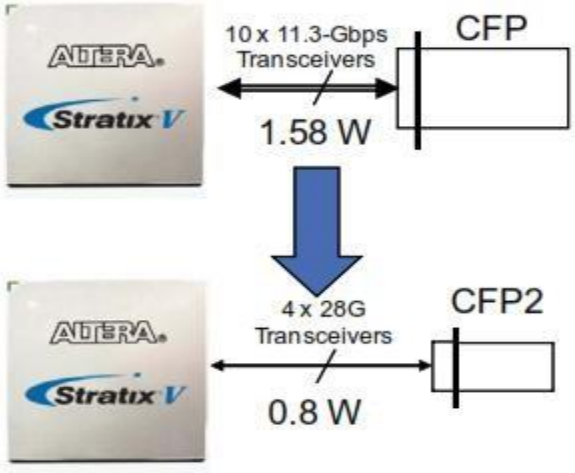

Figure5.Increase Bandwidth and Cut Power by HalfUsing28-Gbps Transceivers

In addition to 28-Gbps transceivers, Stratix V FPGAs integrate power-efficient transceivers withdata rates ranging from 600 Mbps (or 150 Mbps with oversampling) to 14.1 Gbps with best-in-class signal integrity and lowest jitter. Stratix V GX FPGAs offer up to 66 identical power-efficient14.1-Gbpstransceiversthatprovideupto44independentdataratesthroughindependent clock sources. The 28-Gbps and 14.1-Gbps transceivers in Stratix V FPGAs arepower efficient across all supported data rates. Altera took every effort to ensure that transceiversin Stratix VFPGAs deliver therequiredhigh bandwidth or data rate at thelowestpower.Specifically, Altera introduced transceiver power supply banking (see Figure 6) in Stratix VFPGAs, where the transceivers are powered with one of the following power supply voltageoptionsdependingonthetransceiverusageinvariousapplications:

■ Low power (0.85 V) configuration—Used for data rates of Gbps in short reach, chip-to-chip,andchip-to-moduleapplicationswithbasicequalizationtechniques,suchastransmitpre-emphasis/de-emphasisandcontinuoustimelinearequalizer(CLTE).

■ High performance (1.0 V) configuration—Used for noisy and lossy channels, such as long-reachandbackplaneapplicationsatdataratesof>6.5Gbps.Itincludesmoreadvancedequalizationcircuit blocks,suchasdecisionfeedbackequalization(DFE)andautomaticdispersioncompensationengine(ADCE),inadditiontobasiclinearequalizationcircuits.

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■ Off(0 V)—Usedto power downunused transceiversto savepower.

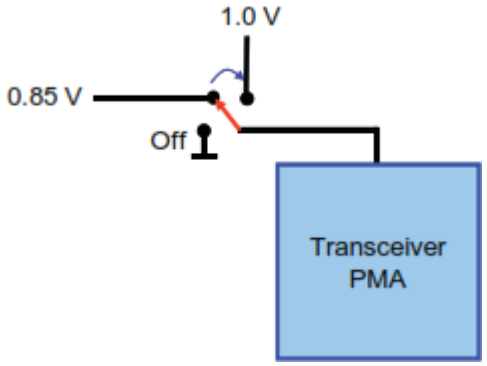

Figure6.ThreePowerSupplyVoltageOptionsforStratixVTransceivers

In addition to transceiver power-supply banking, Altera leveraged various design techniques toensure Stratix V transceivers are power efficient. These techniques include the use of ultra-lowjitter LC-PLL technology supporting low power at the highest data rates in addition to transistorbody biasing to reduce static power, and clock gating to minimize dynamic power. As a result,Stratix V transceivers deliver best-in-class signal integrity performance at the lowest power.Figure 7 shows the transceiver power per channel (blue bars) and the transceiver power pergigabit(redline)forvaryingdataratesonStratixV FPGAs.

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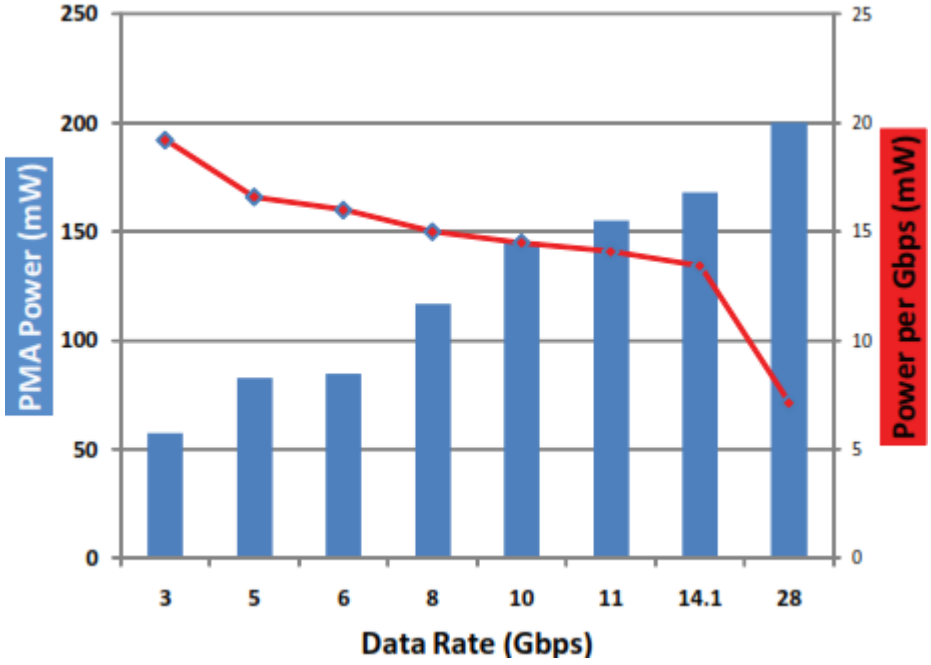

Figure 7.StratixV Transceiver Power per Channel and perGbps

At 28-Gbps, the PMA power per transceiver channel is 200 mW or 7 mW per Gbps. By going tohigher data rates, designers can reduce their system power significantly. For example, to build a10G interface,designers canchooseoneofthefollowing:

■ FourXAUIchannels—Eachrunningat3.125Gbps,consuming240mW

■ One10Gchannel—Runningat10.3125Gbps, consuming145mW, or40%lowerpower

5.CONCLUSION

Power-downandspeed-scaling,forminimizingenergyconsumptionof datatransferunderdeadline and reliability constraints. Both of the problems have been proved to be NP-complete.Altera is addressing the requirements of next-generation applications pushing the limit for higherbandwidthandlowerpowerbyintroducingkeyinnovationson28-nmStratixVFPGAs,including:

■ 28HPprocessinnovations

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■ ProgrammablePowerTechnology

■ Lower voltage(0.85-V)architecture

■ High-bandwidth,power-efficienttransceivers

■ EmbeddedHardCopyBlocksandextensivehardening ofIP

■ Hardpoweringdownoffunctionalblocks

■ I/Oinnovationsenablingpower-efficientmemoryinterfaces

■ QuartusIIsoftwarepoweroptimization

■ LogicandRAMclockgating

■ Fewer powerregulators,switching regulatorsonallsupplies

■ Board-levelintegration:oscillators,decouplingcapacitors,OCT

■ Easy-tousepartialreconfiguration

Altera's comprehensive approach rewards Stratix V customers with many benefits includinghigher performance and lower power FPGA, higher integration through extensive hardening ofIP, and ultimate flexibility through easy-to-use partial reconfiguration. Stratix V FPGAs are theidealdevicesforhigh-endapplicationsrequiringhighbandwidthandlowerpower.

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