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Research Paper

A NOVEL CONTROL SCHEME OF QUASI-RESONANT VALLEY-SWITCHING FOR HIGH-POWER FACTOR AC TO DC LED DRIVERS

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A novel control scheme of Quasi-Resonant (QR) mode and valley-switching for high-Power-Factor (PF) ac-to-dc Light Emitting Diode (LED) drivers. The proposed driver control scheme is based on a buck PF corrector converter, which is operated in QR valley-switching. The proposed control scheme can directly sense the QR valley signal from the current sensor, and it is definitely different from the conventional method which senses the QR valley signal from auxiliary winding. The cost and size of the driver circuit can be remarkably reduced when the proposed control scheme is adopted. Furthermore, the proposed circuit can provide not only high PF and low total harmonic distortion but also high conversion efficiency. Up to 0.99 PF and 91.5% efficiency are obtained from an 8-W (40-W replaced) LED bulb driver prototype.

Keywords: Buck converter, ac to dc converter, LED circuit drive, Power factor corrector, Quasi-resonant, Valley switching

INTRODUCTION

Nowadays, since the improvements in process and technology, the luminous-efficiency of Light-Emitting-Diodes (LEDs) is significantly enhanced. As compared with other light sources, for instance, High Intensity Discharge lamps (HID), Fluorescent Lamps (FL), and Cold Cathode Fluorescent Lamps (CCFL), LED has considerable advantages on mercury-free device, low dc voltage driving, and ultra long lifetime(above 50,000 hours). Due to the international petroleum crisis and greenhouse effect, the whole world looks forward to the more efficient luminaries, and

thus the conventional light sources are progressively replaced by LEDs.

In general, the driver circuit design dominates the energy efficiency as significantly as the light sources. In other words, the lighting product efficiency can be considerably improved via an appropriate driver circuit. Besides, acquiring electrical energy from the wall plugs (ac line voltage source) is the familial way .However, LEDs are more suitable to be driven by dc voltage in accordance with their characteristics, and thus an ac-to-dc conversion stage is necessary. Furthermore, the switching converter is one of

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the most common and efficient LED driving solutions. In general, conventional ac-to-dc switching converters are constructed from a diode-bridge rectifier followed by a bulk capacitor and a dc-to-dc switching converter. This topology has inherent drawbacks, such as the poor performances in power factor and Total Harmonic Distortion (THD) .Therefore, an additional Power Factor Correction (PFC) stage is associated with the current harmonics regulations and improve the power factor at the same time. In spite of its good performance, the two-stage solutions are usually more inefficient and have lower cost/performance (C/P) ratio.

For the sake of improving the above disadvantages and reducing the driver cost, there are several topologies for LED driver circuits that have been developed consequently . Although these LED driver circuits have many advantages, their efficiencies are usually not good enough (about 80%). In order to enhance the power efficiency , the Quasi-Resonant (QR) valley-switching is one of the most familiar methods .The QR valley-switching is achieved by the L-C resonant tank, which is composed of the main inductance and the parasitic capacitance of the power MOSFET. In this way ,the power MOSFET will be switched on once the drain-to-source voltage resonates to the lowest value and to minimize the switching loss, this technique is called valley-switching.

However, the conventional control scheme of QR valley-switching senses the valley signal from an auxiliary winding, as shown in Figure 1, which hinders the magnetic core selection, and further raises the driver cost and size.

PROPOSED BUCK CONVERTER FEEDING LED DRIVES

The proposed system consisting of a bridgeless buck boost converter feeding a BLDC motor drive. The converter is operating in discontinuous inductor current mode for reducing the switching stress. An L filter is used at the input to improve the power quality. A dual buck boost converter is used in which one operating during positive half cycle and the other operating during the negative half cycle. In each of the half cycles, the DC link capacitor is continuously feeding the drive through three different modes. A voltage source inverter is used to provide alternating stator current to the motor drive. Electronic commutation is employed for controlling the switches of inverter so that the speed control of the BLDC drive can be made possible. Power factor correction is done by the voltage feedback control of the converter along with the filter operation. The switching stress will also be evaluated along with the other parameters so that the design of heat sinks can be done easily.

The circuit is operating in three modes in each of the half cycles. Lf and Cf are the filter inductance and capacitance at the input stage. SW1 and Sw2 are the switches, L1 and L2 are

Figure 1 : Proposed Converter
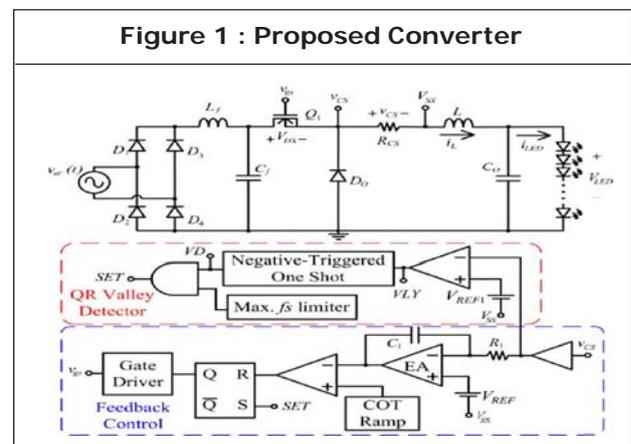
the inductors, D1 and D2 are the diodes in the dual buck boost converter. The inverter switches are numbered through S1 to S6 and the BLDC motor drive employed with hall effect position (Ha-Hc) sensors are also shown in the circuit.

OPERATION ON BUCK CONVERTER

The converter is a dual buck boost converter operating in both positive and negative half cycles of input supply voltage. It is performed in three different modes in each of the half cycles which is given below.

Operation During High Voltage and Low Voltage

Mode 1: In mode 1 q1 is swited on imposing v_{rec} on the inductor L. since L is operated in BCM and DCM to achieve PFC, inductor current i_1, increase linearly from zero and rising slopes of i_L is proportional to the difference of v_{rec} and V_{led}. I_l keeps increasing until Q1 is switched off, at which instant i_L reaches its peak value within the switching cycle.

Mode 2: During this mode of operation, i_L declines the peak contionusly. The downslope of i_L depends on the output voltage, V_{led}. The upload and peak value of i_L is proportional to the difference of V_{rec} and V_{led}. Thus the duration that iL declines to zero varies with V_{rec}. It means that the discharging time of i_L is varied with the BCM and DCM PFC operation, and thus the switching frequency may be varied with V_{rec}. This mode ends when iL, drop to zero and the operation proceed to next mode.

Mode 3: At beginning of this mode, the inductor current i_L has declined to zero. The main inductance L and the parasitic capacitance from a resonant tank. The equivalent circuit is shown in Figure 2. The main inductance L resonant with C_f, the drain-to-source parasitic capacitance diode C_{do} Figure 3 in theoretical waveform

Figure 2: The Operation Equivalent Circuit

(a) Mode I

(b) Mode II

Figure 3: Theoretical Waveform
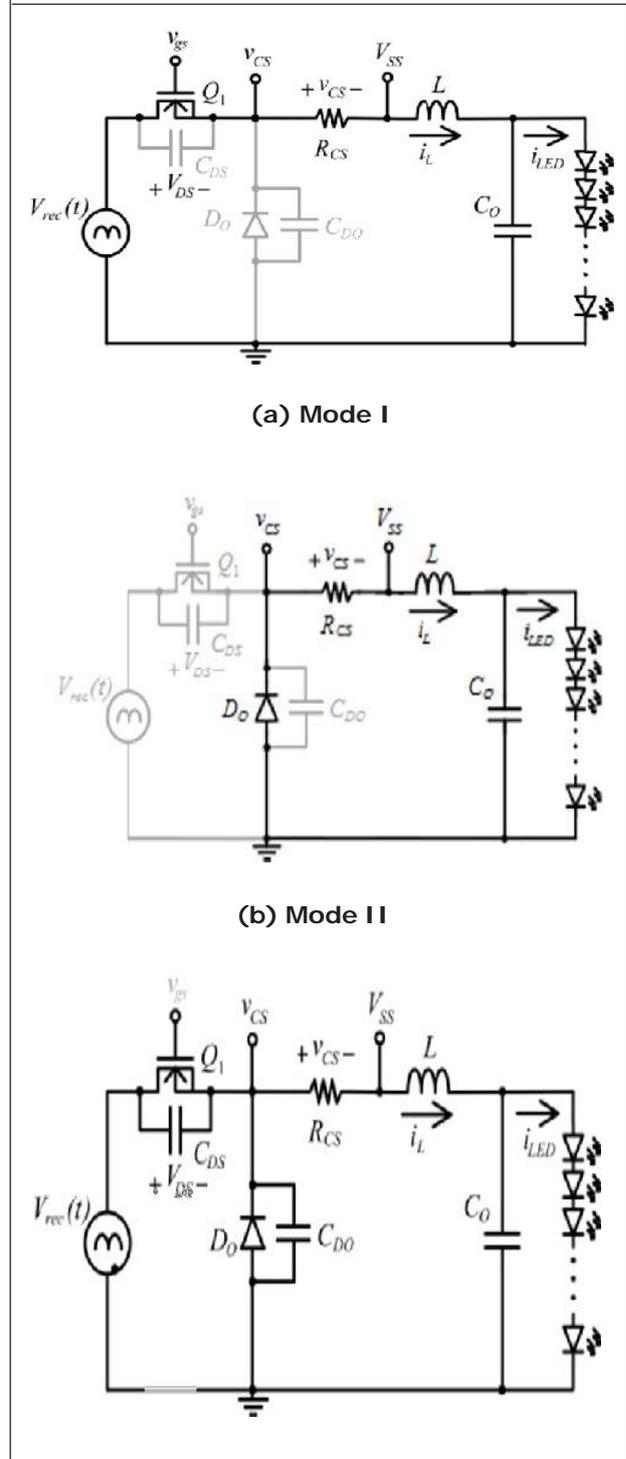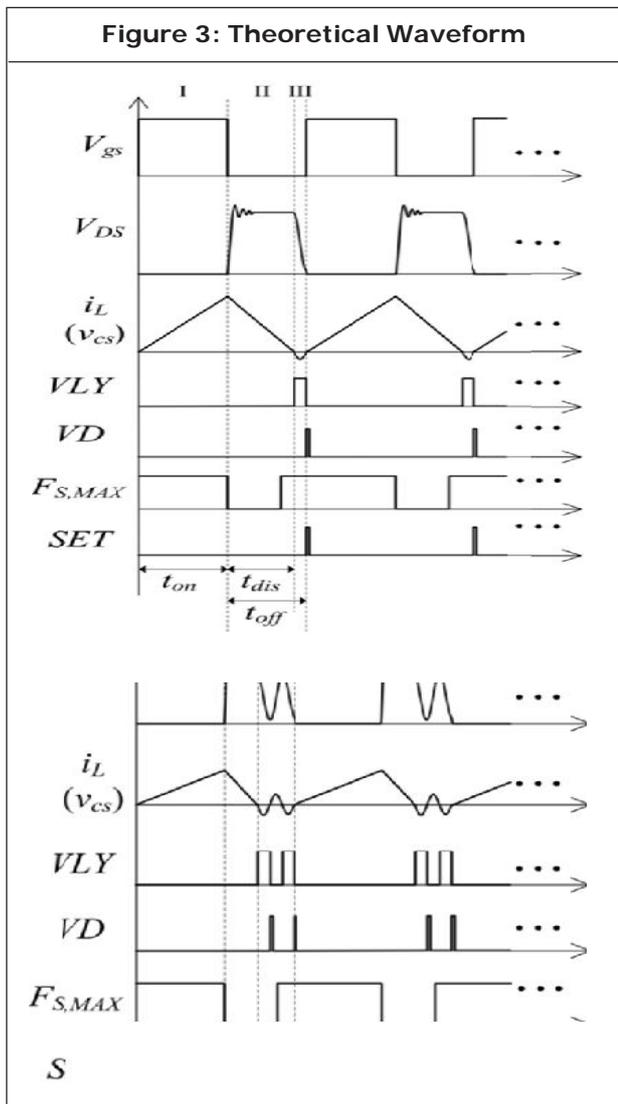
CIRCUIT ANALYSIS

Besides parasitic capacitance of power MOSFET Q1 and freewheeling diode Do, all other component are ideal. The capacitance Cf is small, and the EMI filter is eliminated V_{rec} is purely rectified sinusoidal voltage source. The output capacitance Co is large, so that the Led can be regared as dc voltage. Acoording to the operation principles, this section QR-valley with high power factor ac-to-dc LED driver circuit.

The LED driver circuit supplied by the line voltage source,

$$v_{ac}(t) = V_m \sin(2\pi f_L t)$$

where V_m and f_L are the amplitude and frequency of the line voltage source

The rectified line voltage is,

$$v_{ac}(t) = V_m \sin(2\pi f_L t)$$

Where f_L is much lower than the switching frequency f_s, V_{rec} can be regarded as a dc voltage source over every high-frequency switching cycle of the converter.

Therefore, the buck PFC circuit has to obey the condition as follow.

$$V_{LED} \geq V_{rec}(t). D$$

Due to the proposed circuit is operated in BCM and DCM, i_L increases from zero once Q_1 is switched on and the current reaches its peak at the end of Mode I. It is noted that the line voltage source supplies a current to the buck converter only during Mode II. The rectified input current i_{rec} is equal to i_L when Q_1 is switched on, and the peaks of i_L are enveloped within a sinusoidal in

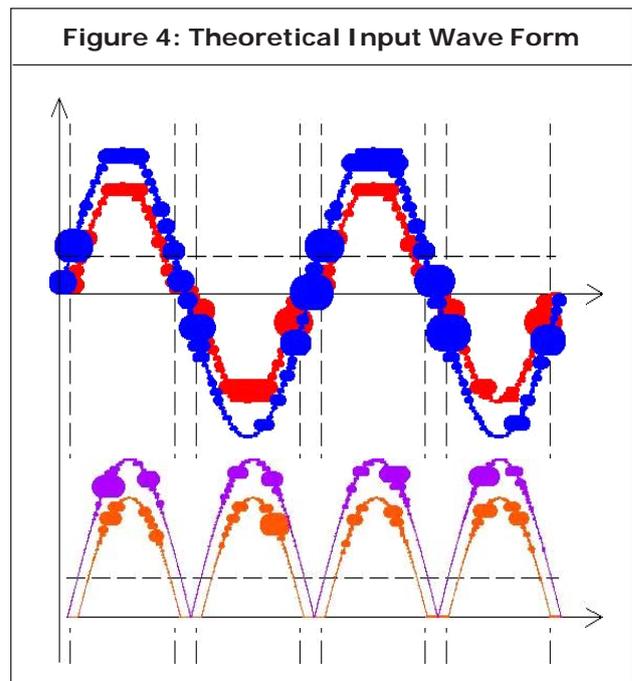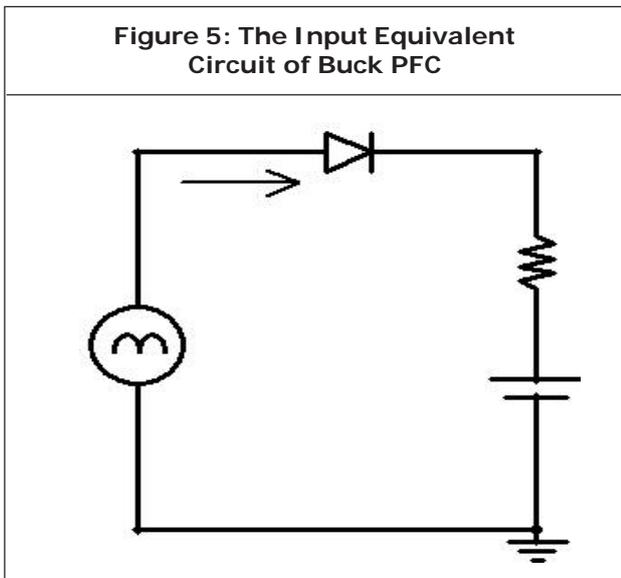**Figure 4: Theoretical Input Wave Form**

**Figure 5: The Input Equivalent Circuit of Buck PFC**

phase to the line input voltage when Q_1 is switched on.

EXPRIMENTAL RESULT

The input EMI filter (Lf and Cf) applied to filter out the switching frequency noise. Although larger Lf and Cf better noise filtering increase the cost and size.

Figure the switching waveform of Vds, iL, and Vgs. The observed waveform prove that the QR-switching valley operations propely without any deviation from the assumption and analysis with the figure and thus the improvement in the circuit efficiency and EMI performance can be achieved. It can be observed that the circuit is approximately operated in BCM at first valley switching (110 V) and the line voltage operated under DCM ar second valley switching (220 V).
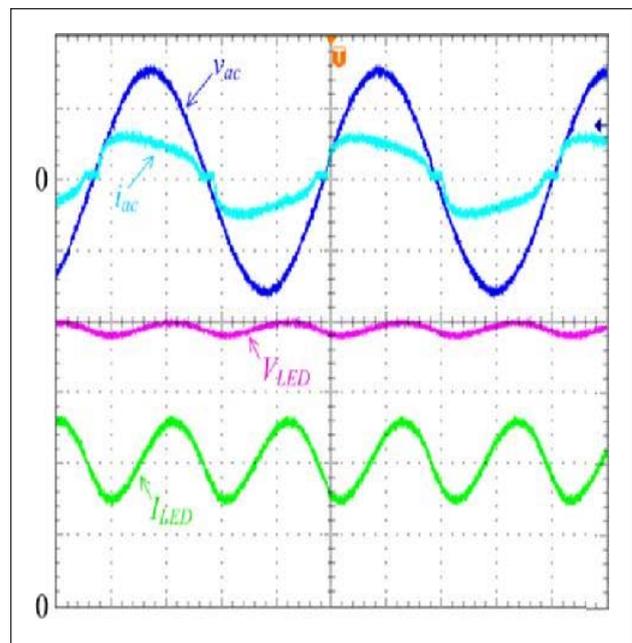
The variation of power factor and circuit efficiency in the Vac range From 85 V rms to 265 V rms. To limit the harmonic content class D device is used when the input power is smaller than 25 W.
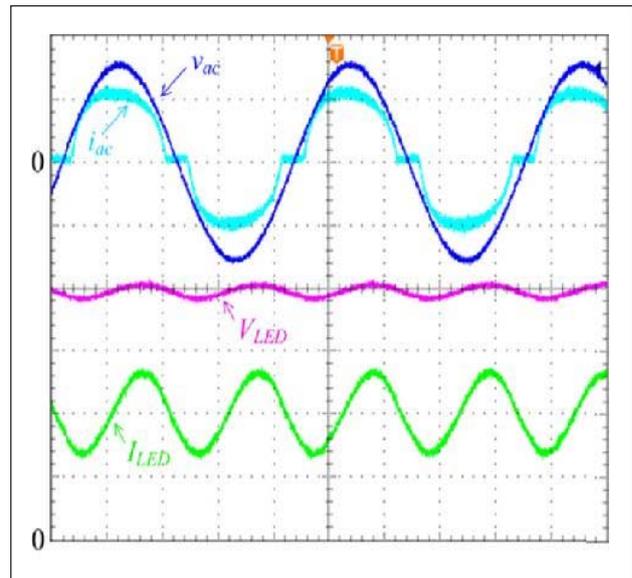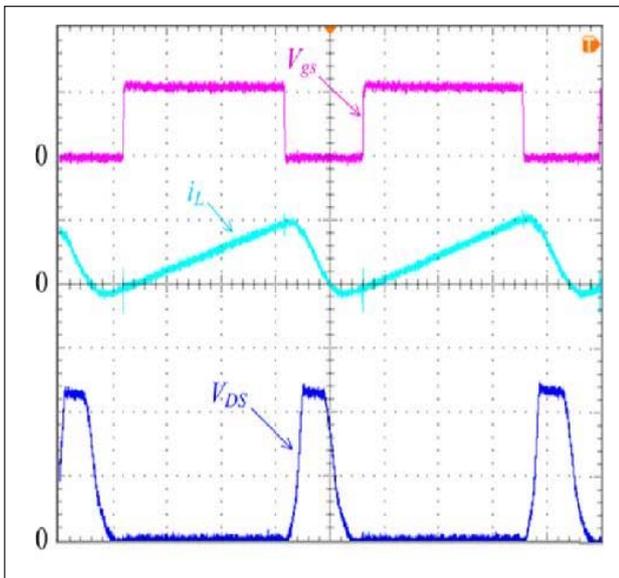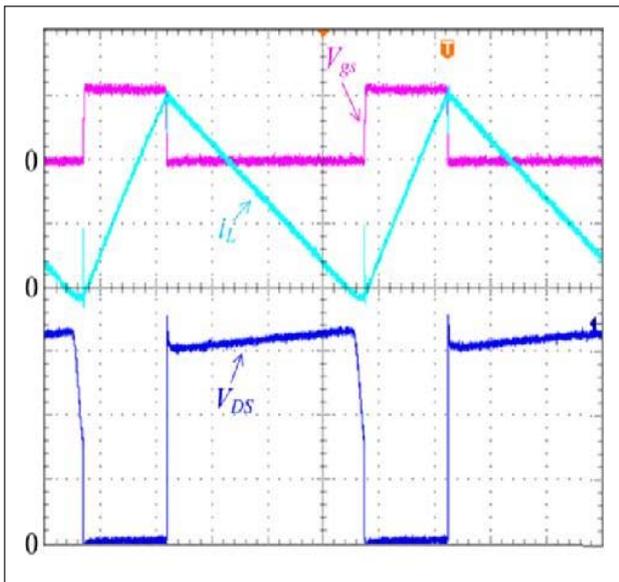

(a) v_{ac} = 110 V_{rms} / 60 Hz

v_{ac}: 100 V/div, i_{ac} :100 mA/ div, V_{LED} : 10 V/div , I_{LED}: 10 0 mA /div , time: 4 ms/div

(b) v_{ac} = 220 V_{rms}/ 60 Hz

v_{ac}: 200 V/div, i_{ac}:10 0 mA/div, V_{LED}: 10V/div, I_{LED}:10 0 m A/div , time:4 ms/div Wave forms of v_{ac}, i_{ac}, V_{LED}, and I_{LED}

Figure: Harmonic Content Reduction

valley switching scheme can dectect the valley from current sense resistance. The auxiliary winding can be eliminated to minimized the core size and cost.

(a) at h igh l ine voltage

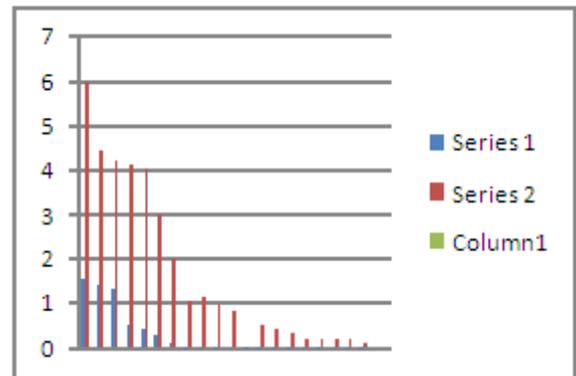V_{DS}: 4 0 V/div, i_L : 20 0 mA /div , V_{gs}: 10V /div , time: 4µ s/di v

(b) at l ow line voltage

V_{DS}: 20 V/ div, i_L: 50 mA /div, V_{gs}: 10 V /div, time: 2 µs/div Wave forms of V_{DS}, i_L, V_{gs} @ v_{ac}= 110 V_{rms}/ 60 H z

SIMULATION RESULTS

The performance of the proposed system of QR-

CONCLUSION

The proposed QR valley-switching scheme can detect the valley from current sense resistance, the auxiliary winding can be eliminated to minimize the magnetic core size and cost. The optimal design of circuit parameters ensures the circuit can achieve the genuine feature of QR valley-switching, leading to a higher efficiency.

A prototype circuit designed for an 8 W LED bulb is implemented and measured to verify the theoretical analyses. The experimental results show that the prototype circuit meets the design targets. Over the universal input line voltage, a power factor higher than 0.93 and a THD less than 23% can be achieved .With the proposed QR valley-switching process, the LED driver circuit achieves a maximum efficiency of 91.5%.

On the other hand, the prototype circuit is just used to validate and demonstrate of the proposed method, and it is implemented in accordance with the commercialized thinking. Therefore, all the control circuit can be easily implement in an

Integrated Circuit (IC) , and thus the cost and size of the final controller would be reasonable and competitive. Moreover, in order to achieve a high power factor, a double-line-frequency ripple is inherent and it could not be eliminated by the proposed control scheme.

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