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Research Paper

POWER EFFICIENT IMPLEMENTATION OF FM0/ MANCHESTER ENCODING ARCHITECTURE

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Dedicated short-range communications are one-way or two-way short-range to medium-range wireless communication channels specifically designed for automotive use and a corresponding set of protocols and standards. In telecommunication and data storage, Manchester coding (also known as phase encoding, or PE) is a line code in which the encoding of each data bit has at least one transition and occupies the same time. The purposes of FM0 and Manchester codes can provide the transmitted signal with dc-balance and are widely adopted in encoding for downlink. The Manchester encoding is realized with a XOR operation for CLK which has a transition within one cycle and input X. The hardware architecture of FM0 encoding should start with the FSM of FM0 first. The DSRC standards generally adopt FM0 and Manchester codes to reach dc-balance, and enhances the signal reliability. The coding-diversity between the FM0 and Manchester codes seriously limits the potential to design a fully reused VLSI architecture. In this paper, the Similarity-Oriented Logic Simplification (SOLS) technique is proposed to overcome this limitation, which improves the hardware utilization rate. In this project Xilinx-ISE tool is used for simulation, logical verification, and further synthesizing.

Keywords: Manchester codes, FM0, SOLS technique, Xilinx-ISE tool

INTRODUCTION

The dedicated short range communication is a protocol for one or two way medium range communication. The DSRC can be briefly classified into two categories: automobile-to-automobile and automobile-to roadside. In automobile-to-automobile, the DSRC enables the message sending and broadcasting among automobile. The automobile-to-roadside focuses

on the intelligent transportation service, such as Electronic Toll Collection (ETC). The DSRC architecture having the transceiver. The transceiver having the baseband processing, RF front end and microprocessor. The microprocessor is used to transfer the instruction to the baseband processing and RF front end. the RF front end is used to transmit and receive the wireless signals using the antenna. The

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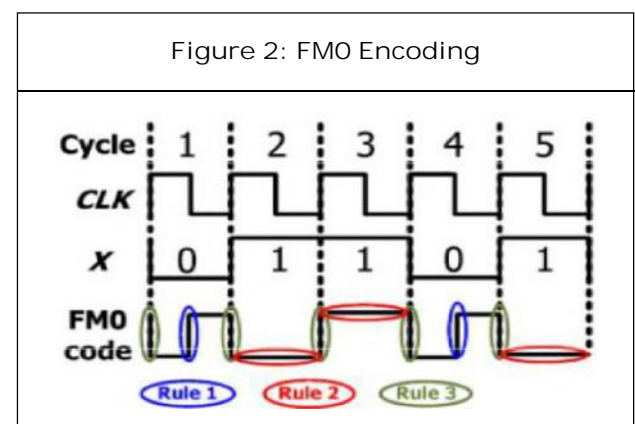
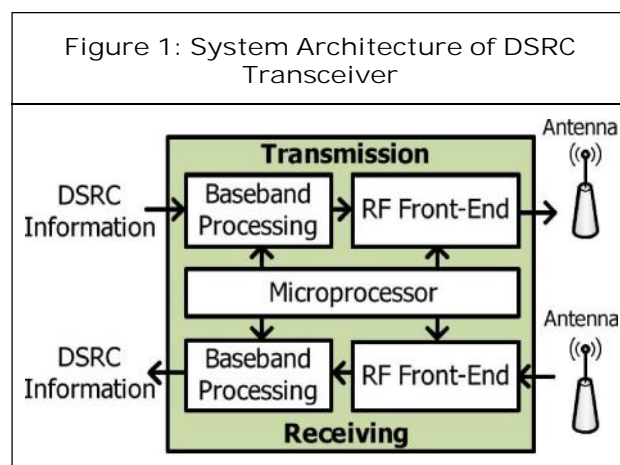
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baseband processing is responsible for modulation, error correction, encoding and synchronization. The transmitted signal consists of the arbitrary binary sequence, it is very difficult to obtain the dc-balance. The FM0 and Manchester are provide the transmitted signal and then the dc-balance. The Similarity Oriented Logic Simplification (SOLS) having the two methods: area compact retiming and balance logic operation sharing. The area compact retiming used to reduce the transistor counts. The balance logic-operation sharing efficiently combines FM0 and Manchester encodings with the fully reused hardware architecture. With SOLS technique, this paper constructs a fully reused VLSI architecture of Manchester and FM0 encodings for DSRC applications. The experiment results reveal that this design achieves an efficient performance compared with sophisticated works.

The DSRC standards have been established by several organizations in different countries. The data rate individually targets at 500 kb/s, 4 Mb/s, and 27 Mb/s with carrier frequency of 5.8 and 5.9 GHz. The modulation methods incorporate amplitude shift keying, phase shift keying, and orthogonal frequency division multiplexing. Generally, the waveform of transmitted signal is expected to have zero-mean

for robustness issue, and this is also referred to as dc-balance. The transmitted signal consists of arbitrary binary sequence, which is difficult to obtain dc-balance. The purposes of FM0 and Manchester codes can provide the transmitted signal with dc-balance. Both FM0 and Manchester codes are widely adopted in encoding for downlink. The VLSI architectures of FM0 and Manchester encoders are reviewed as follows. The system architecture of DSRC transceiver is shown in Figure 1. The upper and bottom parts are dedicated for transmission and receiving, respectively.

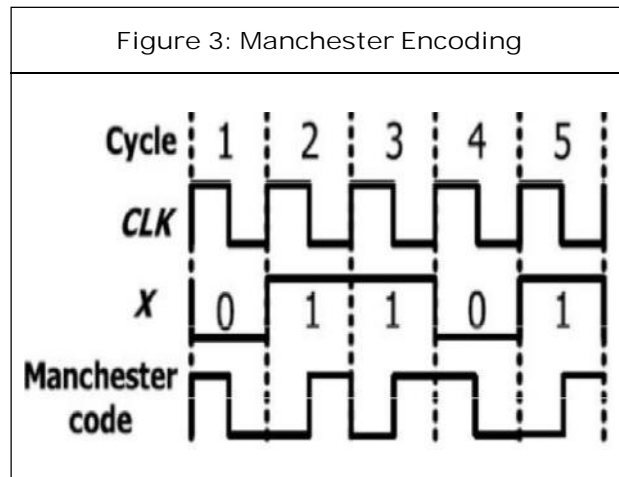
This transceiver is classified into three basic modules: microprocessor, baseband processing, and RF front-end. The microprocessor interprets instructions from media access control to schedule the tasks of baseband processing and RF front-end. The baseband processing is responsible for modulation, error correction, clock synchronization, and encoding. The RF front-end transmits and receives the wireless signal through the antenna. The FM0 having the three rules. If X is the logic-0, the FM0 code has the transition between the A and B. If X is the logic-1. There is no transition is allowed between the A and B. The transition is allocated in each FM0 code. The wave form is given in Figure 2. The FM0 was having the clock and then the x. The



clock and then the cycle having the cycle in each transaction.

Manchester Encoding

The Manchester encoding is realized with the XOR operation for using the CLOCK and X. The clock always has a transition within the one cycle as shown in Figure 3.



DSRC Protocol

Dedicated Short Range Communication (DSRC) is a fast, short to mid range, wireless technology. It enables one way or two way communication between vehicles or between vehicles and roadside. It is used to make streets safer, travel easier and minimize the impact vehicles have on the environment. It provides vehicles and infrastructure the ability to communicate with each other at a rate of 10 times per second. In DSRC communication, the most important concern is collision detection. Each DSRC equipped vehicle broadcasts its basic information including speed, trajectory, location etc to a short range of distance, say a few hundred meters. All other DSRC equipped vehicles in the vicinity receive this message. Later on this message is decoded by the receiver vehicles and a caution or warning may be issued to the driver. This can be issued audibly, visually or haptically.

The DSRC communication is based on direct communication between vehicles and hence does not need networking. Therefore it is also referred to as single hop. This type of communication can also be referred to as uncoordinated broadcast messaging. Each DSRC equipped vehicle can extend this network to its neighbors and hence this network can grow unbounded. In case of safety, privacy is also an important concern. Therefore all safety communications are carried out in the control channel only. The safety communication involves two types of messages. Routine safety messages: These are status messages including change of speed, location, etc that are regularly sent by the vehicle. Event safety messages: These are messages that signify an event like a hard brake.

ARCHITECTURES FOR FMO ENCODER AND MANCHESTER ENCODER

In this paper we propose a VLSI architecture of Manchester encoder for optical communications. We developed a high-speed VLSI architecture almost fully reused with Manchester and Miller encodings for radio frequency identification (RFID) applications. The literature also proposes a Manchester encoding architecture for ultrahigh frequency (UHF) RFID tag emulator. This hardware architecture is conducted from the finite state machine (FSM) of Manchester code, and is realized into field-programmable gate array (FPGA) prototyping system.

The maximum operation frequency of this design is about 256 MHz. The similar design methodology is further applied to individually construct FMO and Miller encoders also for UHF RFID Tag emulator. Its maximum operation

frequency is about 192 MHz. Furthermore, combines Frequency Shift Keying (FSK) modulation and demodulation with Manchester codec in hardware realization. However, the coding-diversity between both seriously limits the potential to design a VLSI architecture that can be fully reused with each other. This paper proposes a VLSI architecture design using Similarity-Oriented Logic Simplification (SOLS) technique.

As shown in Figure 4, for each X, the FM0 code consists of two parts: one for former-half cycle of CLK, A, and the other one for later-half cycle of CLK, B. The coding principle of FM0 is listed as the following three rules.

- 1) If X is the logic-0, the FM0 code must exhibit a transition between A and B.
- 2) If X is the logic-1, no transition is allowed between A and B.
- 3) The transition is allocated among each FM0 code no matter what the X is.

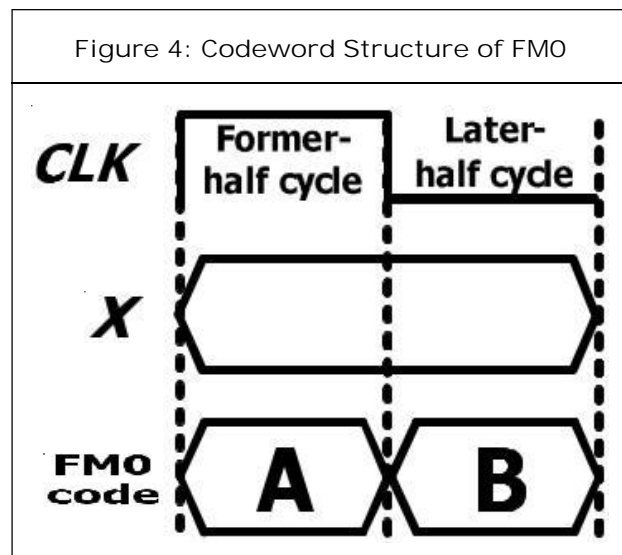
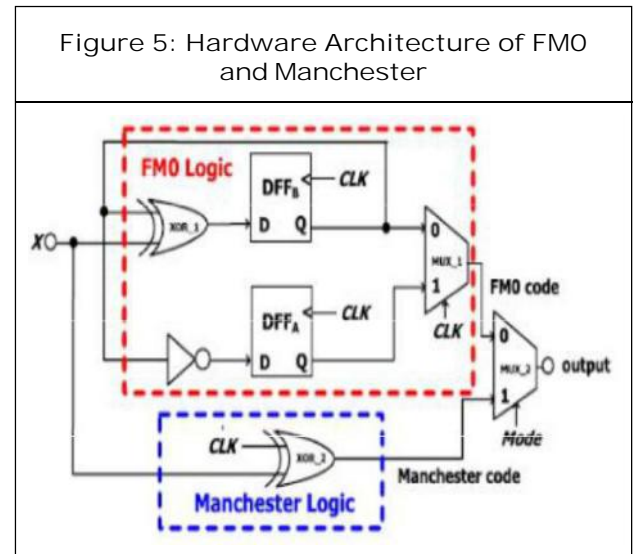


Figure 5 shows the hardware architecture of the FM0/Manchester code. The top part is denoted the FM0 code and then the bottom part



is denoted as the Manchester code. In FM0 code the DFFA and DFFB are used to store the state code of the FM0 code and also mux_1 and not gate is used in the FM0 code. When the mode = 0 is for the FM0 code. The Manchester code is developed only using the XOR gate and when the mode = 1 is for the Manchester code.

The SOLS technique is classified into two parts which are area compact retiming and balance logic operation sharing.

Area Compact Retiming

For FM0 the state code of the each state is stored into DFFA and DFFB .The transition of the state code is only depends on the previous state of B(t-1) instead of the both A(t-1) and B(t-1).

The previous state is denoted as the A(t-1) and then the B(t-1) and then the current state is denoted as the A(t) and then the B(t).

Thus, the FM0 encoding just requires a single 1-bitflip-flop to store the previous value B(t-1).In Figure 6, If the DFFA is directly removed, a non synchronization between A(t) and B(t) causes the logic fault of FM0 code. To avoid this logic-fault,

the DFFB is relocated right after the MUX_1 as shown in Figure 7, where the DFFB is assumed is positive-edge triggered flip flop. At each cycle, the FM0 code, comprising A and B, is derived from the logic of A(t) and the logic of B(t), respectively. The FM0 code is alternatively switched between A(t) and B(t) through the MUX_1 by the control signal of the CLK. In the Q of DFFB is directly updated from the logic of B(t) with 1-cycle latency. When the CLK is logic-0, the B(t) is passed through MUX_1 to the D of DFFB. Then, the upcoming positive-edge of CLK updates it to the Q of DFFB. the timing diagram for the Q of DFFB is consistent whether the DFFB is relocated or not. the B(t) is passed through MUX_1 to the D of DFFB. Then, the upcoming positive-edge of CLK updates it to the Q of DFFB. The timing diagram

for the Q of DFFB is consistent whether the DFFB is relocated or not.

Balance Logic Operation Sharing

The Manchester encoding is derived using the XOR operation. the equation of the XOR gate is given below. The concept of balance logic-operation sharing is to integrate the X into A(t) and X into B(t). The FM0 and Manchester logics have a common point of the multiplexer like logic with the selection of the CLK. The diagram for the balance logic operation sharing shown in Figure 9. The A(t) can be derived from an inverter of B(t - 1), and X is obtained by an inverter of X. The logic for A(t)/X can share the same inverter, and then a multiplexer is placed before the inverter to switch he operands of B(t - 1) and X. The Mode indicates either FM0 or Manchester encoding is adopted.

Figure 6: Encoding Without Area Compact Retiming

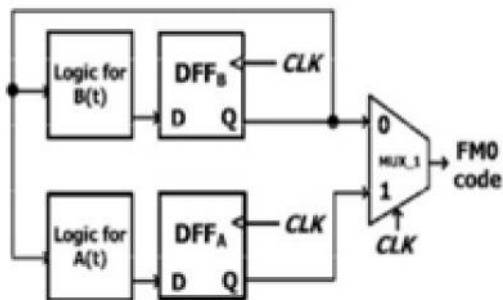


Figure 7: FM0 Encoding with Area Compact Retiming

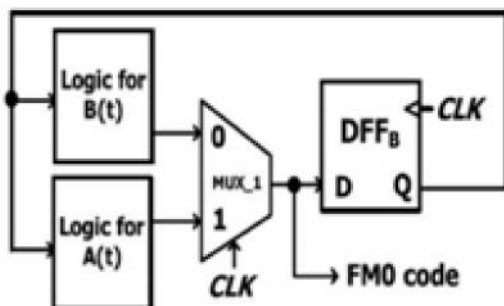


Figure 8: Balance Logic-Operation Sharing of A(t) and X

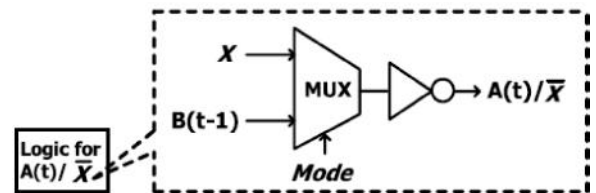


Figure 9: Balance Logic-Operation Sharing of B(t) and X Without the XOR Sharing

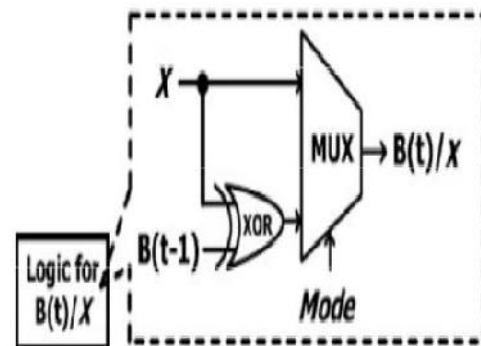


Figure 10: Balance Logic-Operation Sharing of B(t) and X With XOR Sharing

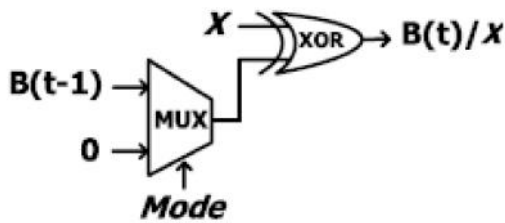


Figure 11: Balance Logic-Operation Sharing of B(t) and X Sharing of the Reused DFFB from Area-Compact Retiming Technique

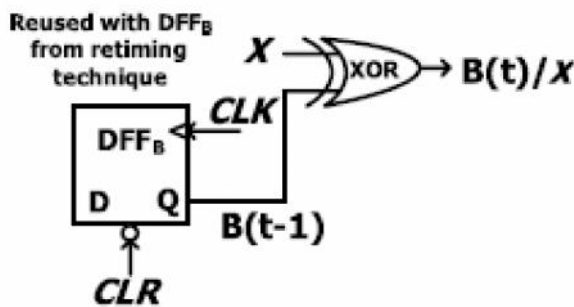
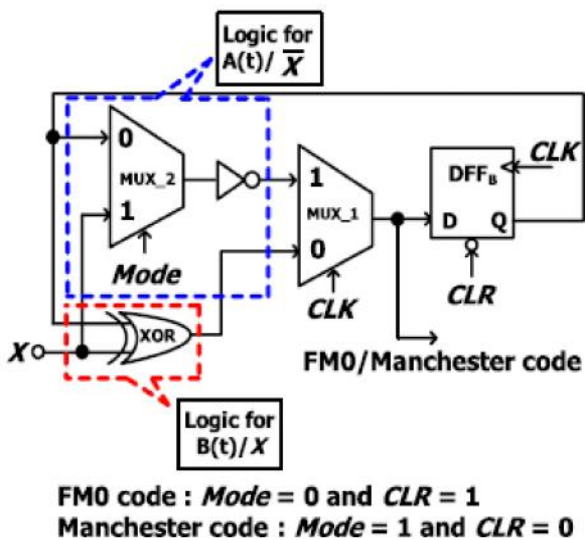


Figure 12: Unbalance Computation Time Between A(t)/X and B(t)/X



The similar concept can be also applied to the logic for B(t)/X, as shown in Figure 8.

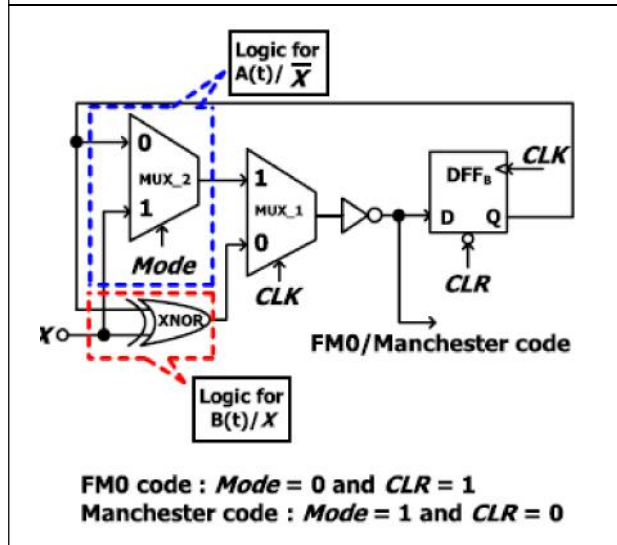
Nevertheless, this architecture exhibits a drawback that the XOR is only dedicated for FM0 encoding, and is not shared with Manchester encoding. The X can be also interpreted as the $A \oplus B$, and thereby the XOR operation can be shared with Manchester and FM0 encodings. As a result, the logic for B(t)/X is shown in Figure 10, where the multiplexer is responsible to switch the operands of B(t-1) and logic-0. This architecture shares the XOR for both B(t) and X. Furthermore, the multiplexer in Figure 10 can be functionally integrated into the relocated DFFB from area-compact retiming technique, as shown in Figure 11. The CLR is the clear signal to reset the content of DFFB to logic-0. The DFFB can be set to zero by activating CLR for Manchester encoding. When the FM0 code is adopted, the CLR is disabled, and the B(t-1) can be derived from DFFB. Hence, the multiplexer in Figure 10 can be totally saved, and its function can be completely integrated into the relocated DFFB.

The logic for A(t)/X includes the MUX_2 and an inverter. Instead, the logic for B(t)/X just incorporates a XOR gate. In the logic for A(t)/X, the computation time of MUX_2 is almost identical to that of XOR in the logic for B(t)/X. However, the logic for A(t)/X further incorporates an inverter in the series of MUX_2. This unbalance computation time between A(t)/X and B(t)/X results in the glitch to MUX_1 as shown in Figure 12, possibly causing the logic-fault on coding.

Unbalance and Balance Computation Time Between A(t)/X and B(t)/X

To alleviate this unbalance computation time, the architecture of the balance computation time between A(t)/X and B(t)/X is shown in Figure 13.

Figure 13: Balance Computation Time Between A(t)/X and B(t)/X



The XOR in the logic for B(t)/X is translated into the XNOR with an inverter, and then this inverter is shared with that of the logic for A(t)/X. This shared inverter is relocated backward to the output of MUX_1. Thus, the logic computation time between A(t)/X and B(t)/X is more balance to each other. The adoption of FM0 or Manchester code depends on Mode and CLR.

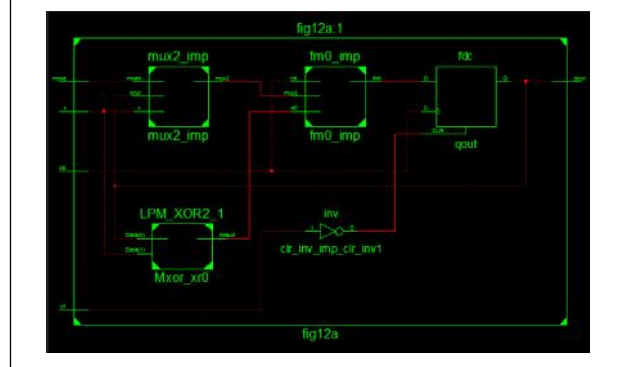
The main differences between this unbalance and balance computation time is buffer insertion whose equivalent figures are shown in Figure 12 and in Figure 13. By placing the buffer the setup violation is fixed but a little bit complexity is introduced. But in most of the circuits where timing is not a big issue there it is used.

RESULTS

RTL Schematic

The RTL SCHEMATIC gives the information about the user view of the design. The internal blocks contains the basic gate representation of the logic. These basic gate realization is purely depend upon the corresponding FPGA selection and the internal database information.

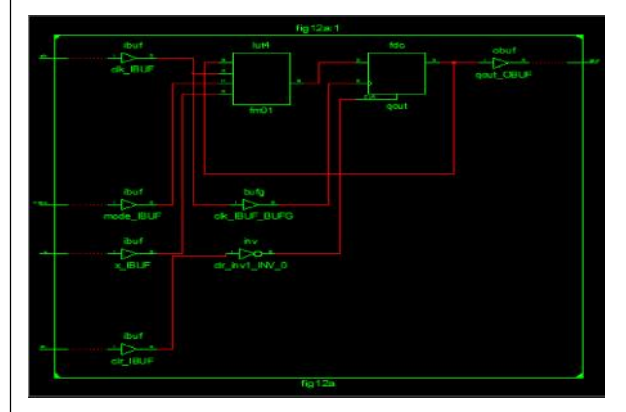
Figure 14: RTL Schematic



Technology Schematic

The Technology Schematic gives the information about the chip view of the design. This mainly consists of LUTs, input buffers, output buffers, D-Flipflop components. Internally Look Up Tables (LUTs) contains the corresponding logic boolean equations, its schematic representation, k-map representation and its truth table representation.

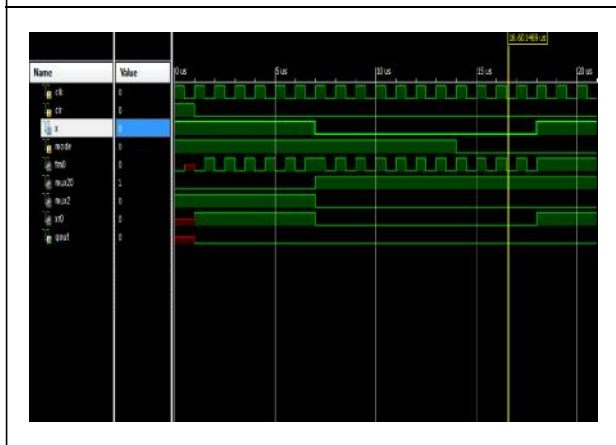
Figure 15: Technology Schematic



Waveform

In the waveform, clk signal represents clock, clr signal represents clear, x signal represents the single bit input which we are applying to the design. All these clk, clr, x signals are inputs. Similarly qout is the output signal for the design. Here clock signal is generated for the positive

Figure 16: Waveform for Unbalance Computation Time Between $A(t)/X$ and $B(t)/X$



edge. Initially the clear signal should be force to logic 1 and after one clock cycle made it to logic 0 for performing the corresponding functional operation. To obtain the required outputs force the inputs logic with the required values.

CONCLUSION

The coding-diversity between FM0 and Manchester encodings causes the limitation on hardware utilization of VLSI architecture design. A limitation analysis on hardware utilization of FM0 and Manchester encodings is discussed in detail. In this paper, the fully reused VLSI architecture using SOLS technique for both FM0 and Manchester encodings is proposed. The SOLS technique eliminates the limitation on hardware utilization by two core techniques: area-compact retiming and balance logic-operation sharing. The balance logic-operation sharing efficiently combines FM0 and Manchester encodings with the identical logic components. Due to the realization of proposed architecture using VERILOG HDL the consumed power is 0.0081 mw only which is very less when compare with the literature survey. The RTL is simulated and synthesized in the XILINX ISE 12.3i.

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