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Research Paper

DESIGN OF PULSE TRIGGERED FLIP-FLOP AND ANALYSIS OF AVERAGE POWER USING PASS TRANSISTOR LOGIC

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Among the various building blocks in digital designs, the most complex and power consuming is the flip-flop. Proper selection of flip-flops is necessary in order to satisfy low power and high performance circuit. In this paper, a novel low power PT-FF design is presented. The paper investigation of conventional and proposed pulse Triggered flip-flop is done with comparisons of average power which claims that proposed design is suitable for low power applications. The proposed design successfully solves the long discharging path problem in conventional explicit type pulse-triggered FF (P-FF) designs and achieves better speed and power performance. The average power consumption and number of transistor count should be reduced by proposed pulse triggered flip-flop design. It will be having much reduced power and area when compared to the other two designs. The performance of the proposed design has been evaluated using Tanner EDA in 130 nm CMOS process technology.

Keywords: Flip flop, Low power, CMOS, Pulse Trigger

INTRODUCTION

A P-FF consists of a pulse generator for strobe signals and a latch for data storage. If they triggering pulses are sufficiently narrow, the latch acts as like an edge triggered Flip Flop. Since only one latch is as opposed to two in the conventional master slave configuration, is needed a Pass transistor FF is simpler in circuit complexity. To obtained balanced performance among power, delay, and area, design space exploration is also as widely used technique. The process variations in the transistor dimensions

and threshold voltage. The proposed framework shows that for a given flip flop design specifications a certain yield can be achieved. To further increases this yield, the proposed frameworks shows which design specifications should be relaxed (Kawaguchi, 1998).

Transistors sizing is rigorously discussed by referring to cases that occur in practical designs. Appropriate metrics with clear physical meaning are proposed and various interesting properties are derived from circuit analysis. A well defined design procedure is derived that can be easily

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automated with commercial CAD tools. Indeed, in realistic pipelined circuits driving the FF has a speed similar to the FF itself and hence the above choice seems more well suited than using a constant slope policy. The average energy is per clock (Chen, 2011).

The effectiveness of the clock optimization slope is discussed the existing classes of FFs. The impact of such an optimization in terms of additive skews and a jitter contribution is discussed, the analysis of the impact of technology scaling. Analysis of the energy contribution in a clock domain has shown that a smoother clock slope leads to an increase in the Flip Flop energy, and a decrease in the energy dissipates by the local clock buffer. A study of the effective technology scaling has revealed that optimization of the clock slope will be more important in the future and that the optimal clock slope will move towards smoother values (Consoli *et al.*, 2012).

Compared to previous papers on Flip Flop comparison the analysis involves that significantly wider range of FF classes and topologies. The extraction of the parasitic capacitances due to local interconnects is a task that must be necessarily accomplished when analyzing nanometer circuits. Therefore, a strategy to estimate the interconnects parasitic as a function of the transistors sizes is essential. The length of these interconnects depend on the relative position of the transistors along their path, as well as the physical dimension of these transistors (Partovi *et al.*, 1996).

Delay in a transistor chain is quadratically proportional to the number of transistors and a signal may degenerate passing through a transistor, buffers are necessary to guarantee

performance and restore signal strength in PTL circuits. In this paper, first analyze effects of buffer insertion on a circuit and give a sufficient and necessary condition for safe buffer insertion. Buffers are implemented by inverters as they are superior in area, timing, and power. Inverter insertion changes a signal to its complement. Furthermore, in the original circuit, a complemented signal may be needed, when passed from one stage to the next stage. Therefore, besides separating long paths into short paths, correct phases must also be decided upon for the whole circuit (Klass *et al.*, 1999).

The decomposition is performed by mapping the BDD to a network flow graph, and then applying the max-flow min-cut technique to bipartition the BDD optimally under a cost function that measures the delay and area of the decomposed implementations. Thus, although the use of PTL may be desired, it remains underutilized and more, because of the lack of good performance-driven synthesis algorithms and methodologies exploiting the properties of PTL circuits. The idea of decomposing logic functions, in general, and

BDD decomposition in particular for optimizing specific objectives is not new, although there is little work on considering PTL-based cost functions during BDD decomposition. Review some of the representative work in the area of Boolean decomposition and BDD decomposition (Stojanovic, 1999). The main idea is to adopt a push-pull output stage, which is driven by two split paths for rise and fall output transitions with the explicit aim of reducing both the path effort and the parasitic delay. In addition, the capacitance at the output of the first stage is

further reduced by adopting half-latches in the split paths and moving the cross-coupled inverters to the output node (Tschanz, 2001).

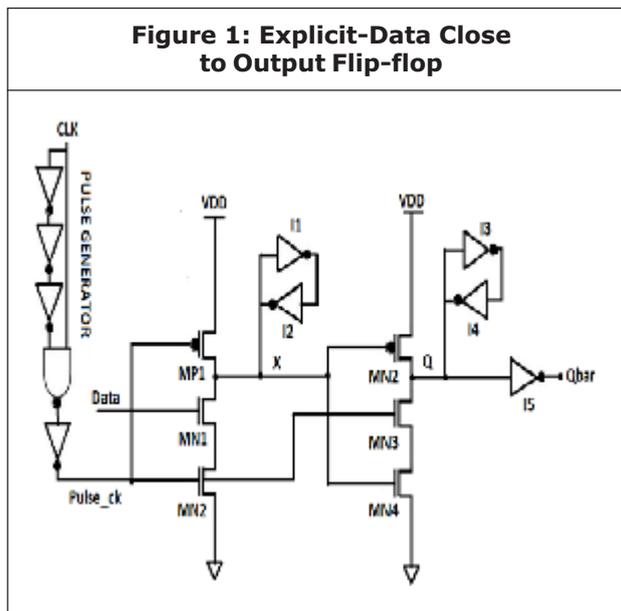
EXISTING METHOD

In an implicit type P-FF, the pulse generator is part of the latch design and no explicit pulse signals are generated. However, they suffer from a longer discharging path, which leads to inferior timing characteristics. Explicit pulse generation, on the contrary, incurs more power consumption but the logic separation from the latch design gives the FF design a unique speed advantage. To overcome this problem, many remedial

in the conventional power generations such as decreasing reserves and adverse effect on the environment. Among all the renewable energy sources the contribution of the Wind Energy Conversion System (WECS) is effective and it is reliable energy resource.

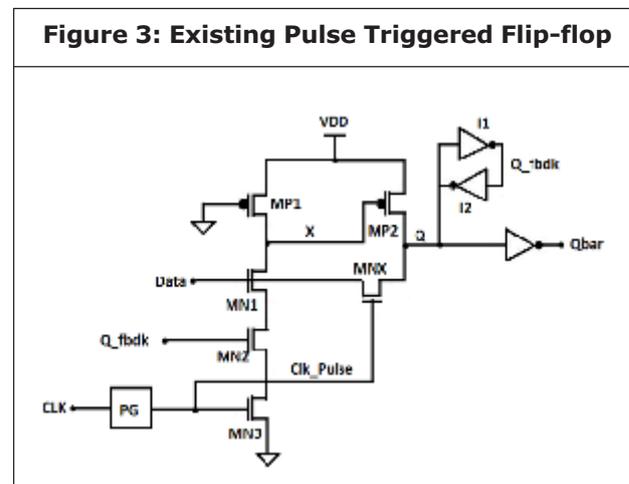
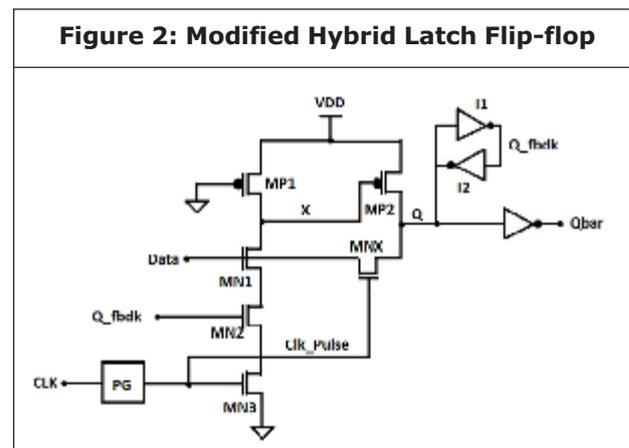
MODIFIED PULSE TRIGGERED DESIGN

The existing pulse triggered flip-flop, a novel P-FF design by employing a modified TSPC latch structure incorporating a mixed design style consisting of a pass transistor and a pseudo-nMOS logic. The key idea was to provide a signal feed through from input source to the internal node of the latch, which would facilitate extra driving to shorten the transition time. Similar to



measures such as conditional capture, conditional precharge, conditional discharge, and conditional pulse enhancement scheme have been proposed.

A control strategy for Doubly Fed Induction Generator in which stator is directly connected to grid, but the rotor terminals are connected to grid via power converter in Figure 2. The need for renewable energy sources for electric power generation has been increased due to limitations



the SCDF design, the PFF design also employs a static latch structure and a conditional discharge scheme to avoid superfluous switching at an internal node.

First, a weak pull-up pMOS transistor MP1 with gate connected to the ground is used in the first stage of the TSPC latch. This gives rise to a pseudo-nMOS logic style design, and the charge keeper circuit for the internal node X can be saved. In addition to the circuit simplicity, this approach also reduces the load capacitance of node. Second, a pass transistor MNx controlled by the pulse clock is included so that input data can drive node Q of the latch directly (the signal feed-through scheme). Along with the pull-up transistor MP2 at the second stage inverter of the TSPC latch, this extra passage facilitates auxiliary signal driving from the input source to node Q. The node level can thus be quickly pulled up to shorten the data transition delay. Third, the pull-down network of the second stage inverter is completely removed. Instead, the newly employed pass transistor MNx provides a discharging path. The role played by MNx is thus twofold, i.e., providing extra driving to node Q during 0 to 1 data transitions, and discharging node Q during "1" to "0" data transitions. Compared with the latch structure used in SCDF design, the circuit savings of the proposed design include a charge keeper (two inverters), a pull-down network (two nMOS transistors), and a control inverter. The only extra component introduced is an nMOS pass transistor to support signal feed through.

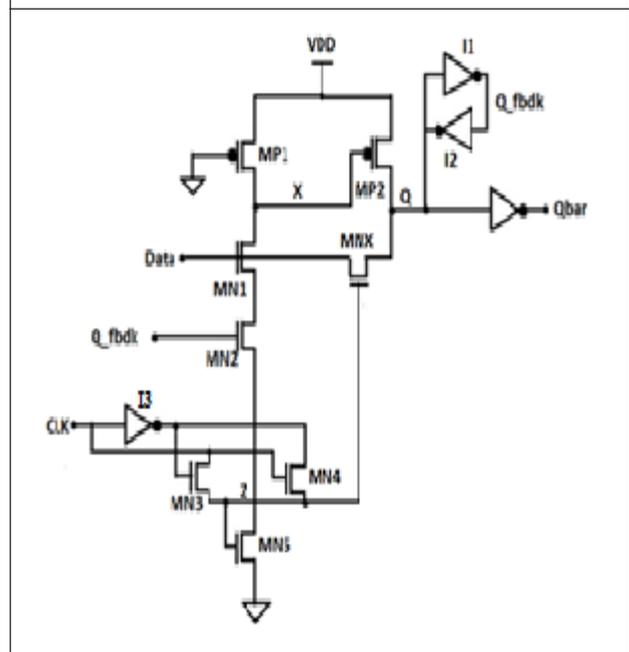
PROPOSED PULSE TRIGGERED DESIGN

The Proposed pulse triggered flip-flop design shown in Figure 4 which employs a static latch structure and at two-input Pass Transistor Logic

(PTL)-based AND gate is implemented with nMOS pass transistor in existing pulse triggered with signal feed through scheme. By using the PTL family idea we are designing this circuit as well as by using the pass transistor logic we are using only one clocking transistor so it will be consuming only less power in the clock network of the flip-flop when compared to all other circuits. As well as proposed pulse triggered flip-flop having only 16 Transistors.

The clocking transistor is used to control the charge of transistor MN5. Since the two inputs to the AND logic are mostly complementary (except during the transition edges of the clock), the output node Z is kept at zero most of the time. At the rising edges of the clock, both transistors MN3 and MN4 are turned on and collaborate to pass a weak logic high to node Z, which then turns on transistor MN5 by a time span defined by the delay inverter I3. The switching power at node Z can be reduced due to a diminished voltage swing.

Figure 4: Proposed Pulse Edge Trigger Flip Flop Simulation Results

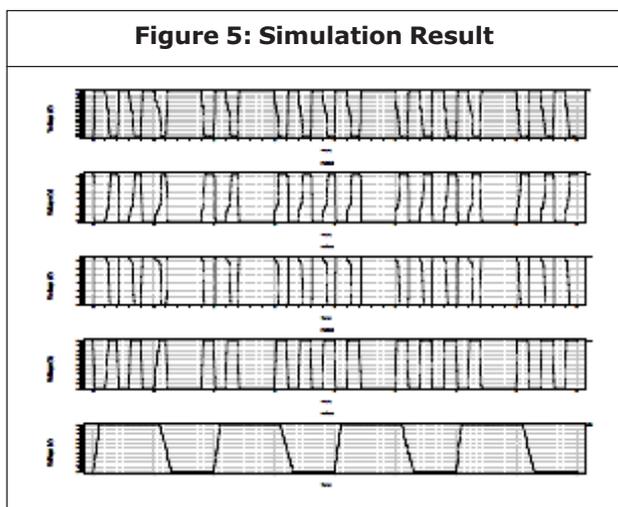


When a clock pulse arrives, if no data transition occurs, i.e., the input data and node Q are at the same level, no current passes through the pass transistor MN_x, which keeps the input stage of the FF from any driving effort. If a “0” to “1” data transition occurs, node X is discharged to turn on transistor MP₂, which then pulls node Q high. Since a keeper logic is placed at node Q, the discharging duty of the input source is lifted once the state of the keeper logic is inverted.

The simulation is performed for various pulse triggered flip-flops such as explicit data close to output and modified hybrid latch flip-flop design to demonstrate the effectiveness of our proposed design.

SIMULATION RESULT

The exception is the MHLFF design, which has a slightly positive setup time and a shorter hold time than its counterparts because of a simpler pulse generator. A longer hold time mainly affects the design of the driving logic. If P-FFs are adopted in the entire design, the hold time constraint can be easily satisfied because of a prolonged clock-to-Q delay property in P-FF designs. Introducing an input delay buffer is also a simple measure to alleviate the hold time requirement.



CONCLUSION

The proposed pulse triggered flip-flop is designed with two-input PTL-based AND gate is implemented in existing pulse triggered flip-flop with signal feed through scheme of pseudo n-MOS logic pass transistor. This design is combination of conditional pulse enhancement scheme and existing pulse triggered flip-flop with signal feed through scheme. The average power consumption and number of transistor count should be reduced by proposed pulse triggered flip-flop design. It will be having much reduced power and area when compared to the other two designs. At the same time due to the reduced no of transistor count we can reduce the delay oriented things also. Thus we are reducing the overall switching delay and power, area consumption. So, this circuit will be acting as good sequential elements when compared to other flip-flop design. The performance of the proposed design has been evaluated using HSPICE in 0.18 μm CMOS process technology. In future work of the paper, the embedded logic function will be design and implement using proposed pulse triggered flip-flop design. To analysis and reduces the average and leakage power consumption of the embedded based logic function of pulse triggered flip-flop design and to achieve high performance pulse triggered flipflop design.

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