International Journal of Engineering Research and Science & Technology

ISSN : 2319-5991
Vol. 4, No. 1
February 2015

www.ijerst.com

Email: editorijerst@gmail.com or editor@ijerst.com

International Journal of Engineering Research and Science & Technology

ISSN 2319-5991 www.ijerst.com
Vol. 4, No. 1, February 2015

Research Paper

A PASS TRANSISTOR BASED D FLIP-FLOP DESIGN USING NEGATIVE EDGE TRIGGERED CIRCUIT

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A new technique is proposed based on the comparison between Conventional Transistorized Flip flop and Data transition Look ahead D flip flop here we are checking the working of DLDFF and the conventional D Flip-flop after that we are analyzing the characteristic comparison using power & area constraints after that we are proposing a Negative Edge triggered flip-flop named as Switching Transistor based D Flip-Flop (STDFF) with reduced number of transistors which will reduce the overall power area as well as delay. The simulation is done by using Tanner EDA analysis software tools and the result between all those types is under 130 nm technology. In that our proposed system is shows better output than the other flip flops compared here. If the input is idle, then the proposed design D Flip-flop saves up to 85% of the power when compared with the Auto Gated method.

Keywords: STDFF, D Flip Flop, Negative Edge trigger, Conventional Transistor

INTRODUCTION

The widespread use of mobile devices in modern society, power efficiency and energy savings become extremely important issues for designer. Normally high performance chips have high integration density and high clock frequency which tends to dictates the power consumption. The design method is needed that consume less power while maintaining the comparable performance method. Power consumption is the conventional CMOS digital circuit can be separated into three types of power dissipation: (i) switching power, (ii) short-circuit power, and (iii) leakage power consumption. The switching power the power dissipation during the signal transitions, when the energy is drawn from the power supply to charge-up the device capacitances. The short circuit power is produced during the moment that both the PMOS network and the NMOS network are simultaneously on in CMOS logic. A data driven methods stop most of those and yields high power savings, but it's implementation is very complex and applications dependent. A third methods called auto gated Flip flops, is simple but yields relatively small power savings. This process combines all the three

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methods, LACG computes the clock enabling signals of each Flip-flop of one cycle ahead of time, based on present cycle (Oklobdzija, 2003). The flip-flop has one enable input that allows for both Positive and Negative Edge Triggered (PET and NET) operation without changing the design of the circuit. It is mainly reconfigurable by design; numerical simulation has been conducted to assess the performance of the circuit. The outputs from both bar and cross ports of the device have been utilized (Benini, 2000).

A conventional master-slave flip-flop is very sensitive to particle strike when the clock is high, that causes a SEU may upset the logic state of the master latch resulting in a faulty output of the flip flop, and the erroneous value will also been locked in the slave latch when clock is low. When the clock signal is high or low the SEU is the Master or Slave latch of a flip flop can be detected by the error detections circuit using dynamic logic method. The mux selects a correct output according to the error indication signal. The proposed flip flop has small area, power and delay overheads and good radiation hardening capabilities. A multiplexer is used to select the correct value as final output according to the fault indication signal (Hosny and Yuejian, 2008). Expressions for the power savings in a gated clock tree are presented and the optimal grater fan out is derived, based on the flip flop toggling probabilities, process technique parameters. The resulting clock gate methods achieve the 10% savings for the total clock tree switched power. The timing implication of this proposed gating scheme is discussed. The grouping of the FF's for a joint clock gating is also be discussed (Chunhong *et al.,* 2002).

To present a high speed method, wide range of parallel counter that achieves high operating frequencies through a novel pipeline partitioning methodology using only three simple repeated CMOS logic module types: an initial module generates anticipated counting states for higher significant bit modules through the state look ahead path, simple D type flip flops and 2 bit counters. The state look ahead path prepares the counting path's next counter state prior to the clock edge such that the clock edge triggers all modules simultaneously, thus concurrently updating the count state with a uniform delay at all counting path modules/stages with respect to the clock edge (Farrahi *et al.,* 2001).

When a thread gets blocked due to a memory stall, the corresponding register file can be placed in a low leakage state through power gating for leakage reduction. When the memory stall gets resolved, the register file is activated for being accessed again. Since the contents of the register file are not lost and restored on wakeup, this is referred to as state-retentive power gating of register files. While state-retentive power gating in single cores has been studied in the literature, it is being investigated for multicore architectures for the first time in this work. Each technique uses two different modes of leakage states: low leakage savings and low wake-up and high-leakage savings and high wake-up latency. The overhead due to wake-up latency is completely avoided in two techniques while it is hidden for most part in the third approach, either by overlapping the wake-up process with the thread context switching latency or by executing instructions from other threads ready for execution (Shen *et al.,* 2008).

Clock gating design at RTL is coarse and it pays no attention to the physical information, therefore, it often results in large wire length overhead. While the clock gating is considered only at clock tree synthesis, the optimization

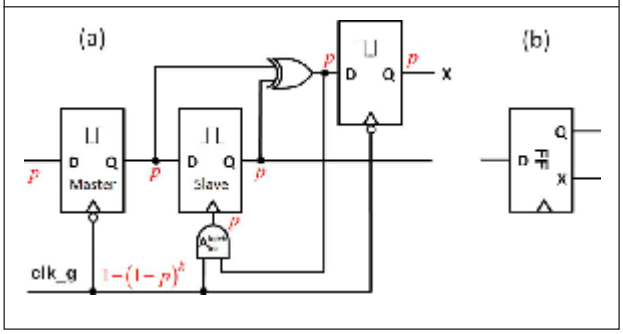
space is largely limited due to the fixing of registers. To fully use the logical and physical information between registers, we propose a new flow for low-power gated clock tree design in this work. It mainly includes three parts: gated clock tree aware register placement, gated clock tree construction, and incremental placement. Compared with the previous works on clock gating, our algorithm reduces the clock tree power with much fewer gating logics, the overhead to the placement is also reduced (Synopsis, 2010).

Two essential problems to be dealt with in the design of look-ahead filters are stability and computational complexity of the filter. In this paper, a new periodic scheme is proposed to stabilize the-step look-ahead filter and provide minimum amount of computation in digital implementation of the filter (Wimer and Koren, 2012). LAMB maximizes the number of users admitted in a window, which includes the reneging time of all pending requests at that scheduling time. LAMB admits a greater number of users than other existing batching policies. Furthermore, the benefit of integrating batching and piggybacking is analyzed. This window is lower bounded by the reneging time of a user who is about to leave the system and upper bounded by the most distant reneging time of a user waiting to be served For high capacity servers, LAMB admits the greatest number of users of all Max Batch policies (Donno, 2004).

AUTO-GATED FLIP-FLOPS

Clock gating method is a very useful method for to reduce the flip flops. A data driven method stops most of those and higher field yields higher power savings. It avoids the tight timing constraints of AGFF and data-driven by allotting a full clock cycle for the computation of the enabling signals and their propagation. A closed-form model characterizing the power saving per FF is presented. To maximize the power savings, the FFs should be grouped such that their toggling is

Figure 1: Auto Gated Flip Flop



highly correlated. This requires running extensive simulations characterizing the typical different versions of the same IP.

CLOCK GATING

Clock gating is very useful for reducing the power consumed by digital systems. A data-driven method stops most of those and yields higher power savings, but its implementation is complex and application dependent. A third method called auto gated FFs is simple but yields relatively small power savings. Ordinarily when a logic unit is clocked its underlying sequential elements receive the clock signal regardless of whether or not their data will toggle in the next cycle signal regardless of whether or not their data will toggle in the next cycle. With clock gating the clock signals are ended with explicitly predefined enabling signals.

LOOK AHEAD CLOCK GATING

It computes the clock enabling signals of each FF one cycle ahead of time, based on the present

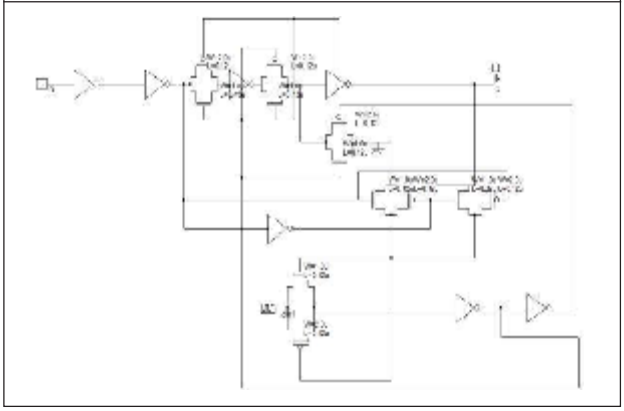
cycle data of those FFs on which it depends. Similarly to data-driven gating, it is capable of stopping the majority of redundant clock pulses. Look-Ahead Clock Gating (LACG) computes the clock enabling signals of each FF one cycle ahead of time, based on the present cycle data of those FFs on which it depends. Similarly to data-driven gating, it is capable of stopping the majority of redundant clock pulses. It has however a big advantage of avoiding the tight timing constraints of AGFF and data-driven clock gating.

PROPOSED METHOD

Pass Transistor Based Negative Edge Trigged D Flip Flop

The comparison between Conventional Transistorized Flip-flop and Data transition Look ahead D flip flop the working of DLDFF and the conventional D Flip-flop after that we are analyzing the characteristic comparison using power and area constraints after that we are proposing a Negative Edge triggered flip-flop named as Pass transistor based negative edge trigged D Flip Flop (PTDFF) with reduced number of transistors which will reduce the overall power area as well as delay. The circuit can be made to change state by signals applied to one or more control inputs and will have one or two outputs. It is the basic storage element in sequential logic.

Figure 2: Clock Gating Flip Flop



Conventional Low Power D Flip-Flop

Flip-Flops are the basic elements for storing information and they are the fundamental building blocks for all sequential circuits. Flip-flops have their content change only either at the rising or falling edge of the enable signal.

DLDFF

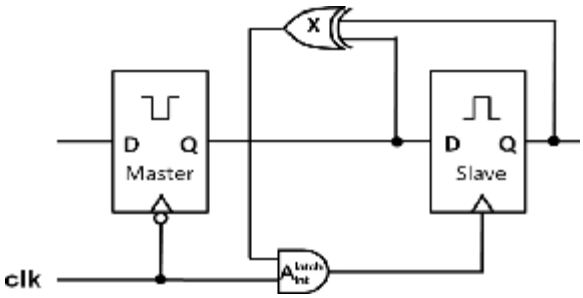
The gating function is derived within the flip flop without any external control signal. The external clock signal of the flip-flop still switches. But, the clock signal flowing into the flip flop is deactivated when there are no data transitions.

EXPERIMENTAL RESULTS

Existing Model

The gating scheme presented was first verified by a formal verification EDA tool and it was found equivalent to the original circuit before the gating logic was introduced. Though not surprising, it is a must in an industrial environment where the method was experimented. It is important to note that the introduction of LACG made most of the gate-level clock gating techniques employed by this design redundant.

Figure 3: Existing Circuit



Another difficulty of data-driven gating is its design methodology. To maximize the power

savings, the FFs should be grouped such that their toggling is highly correlated. This requires running extensive simulations characterizing the typical applications expected by the end-user the embedding of LACG logic in the RTL functional code is uniquely defined and easily derived from the underlying logic, independently of the target application.

Proposed Circuit

In this method the circuit has been designed using the tool of Tanner EDA software130 nm technology. The circuit helps to reduce the circuit area and power circuit.

Based on the data to clock toggling probability, a model to derive the group size maximizing the power savings was developed. A comparison between the synthesis-based and data-driven gating methods showed that the latter outperforms for control and arithmetic circuits, while the former outperforms for register.

There, the clock signal driving a FF, is disabled (gated) when the FF's state is not subject to change in the next clock cycle In an attempt to reduce the overhead of the gating logic, several FFs are driven by the same clock signal, generated by the enabling signals of the individual. Data-driven gating is illustrated. FF finds out that

Figure 4: Tanner Based Circuit

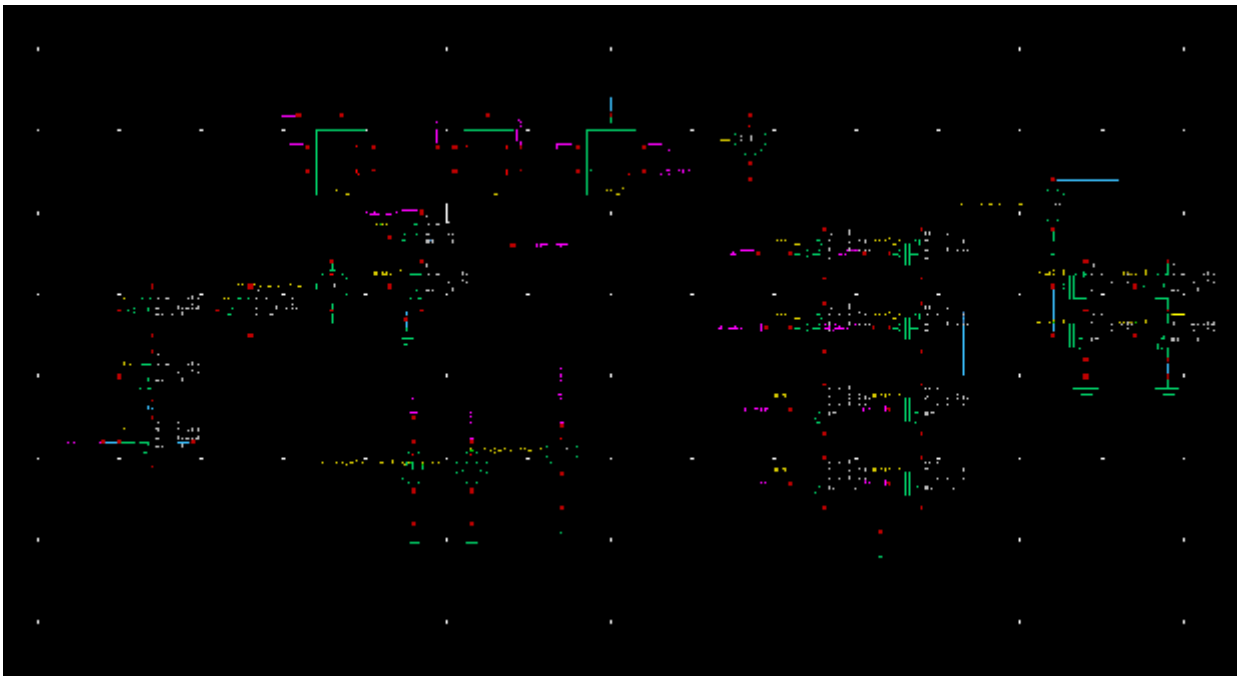
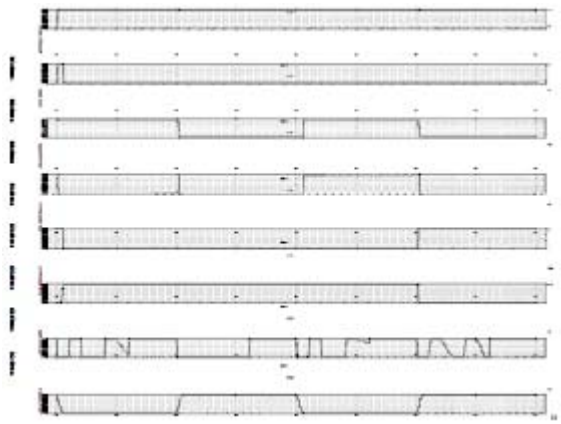


Figure 5: Circuit Graph



its clock can be disabled in the next cycle by its output with the present input data that will appear at its output in the next cycle.

CONCLUSION

A new D Flip flop design which is named as Pass transistor based negative edge trigged D Flip Flop (PTDFF). The Proposed system shows 85% Power improvement than the Existing Data Transition look ahead D Flip-Flop and it shows an improvement of 40% in area constraints. Thus our proposed system is having very less power and area constraints which will lead to improvement in the case implementation in future mobile devices. This can be much suitable for application of battery oriented operation for less power and area. In future we can add some other leakage reduction techniques and the power can be further reduced. Look-ahead clock gating has been shown to be very useful in reducing the clock switching power. The computation of the clock enabling signals one cycle ahead of time avoids the tight timing constraints existing in other gating methods. A closed form model characterizing the power saving was presented and used in the implementation of the gating logic. The gating logic can be further optimized by matching target FFs for joint gating which may significantly reduce the hardware overheads.

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