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Research Paper

DESIGN AND ANALYSIS OF LOW POWER PARALLEL SELF TIMED ADDER USING RADIX METHOD

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The addition of two binary numbers is the fundamental and most often used arithmetic operation on microprocessors, Digital Signal Processors (DSP), and data-processing Application-Specific Integrated Circuits (ASIC). Therefore, binary adders are crucial building blocks in Very Large-Scale Integrated (VLSI) circuits. Their efficient implementation is not trivial because a costly carry propagation operation involving all operand bits has to be performed. Many different circuit architectures for binary addition have been proposed over the last decades, covering a wide range of performance characteristics. In this brief, an efficient implementation of asynchronous parallel adder. It is based on Radix method for faster computation of sum and reduced delay. It is a recursive formulation for performing multi bit binary addition. The computation has been carried out using parallel processes. Radix-2 is reduce the Power Delay Product (PDP) and Energy Delay Product (EDP).To obtain low area, the carry is generated first and then it is reused in sum generation. The adder is Implemented using Tanner tool. The practicality and superiority of the proposed technique have been verified by simulation.

Keywords: Processor, ASIC, Power Delay Product, Energy Delay Product, Tanner

INTRODUCTION

Over the past few decades, low power design solution has steadily geared up the list of researcher's design concerns for low power and low noise digital circuits to introduce new methods to the design of low power VLSI circuits. Moore's law describes the requirement of the transistors for VLSI design which gives the experimental observation of component density and performance of integrated circuits, which doubles every two years. Transistor count is a primary concern which largely affects the design complexity of many function units such as multiplier and Arithmetic Logic Unit (ALU). The significance of the digital computing lies in the multiplier design. The multipliers play a significant role in arithmetic operations in DSP applications. Recent developments in processor designs also focus on low power multiplier architecture usage in their circuits. Two significant yet often

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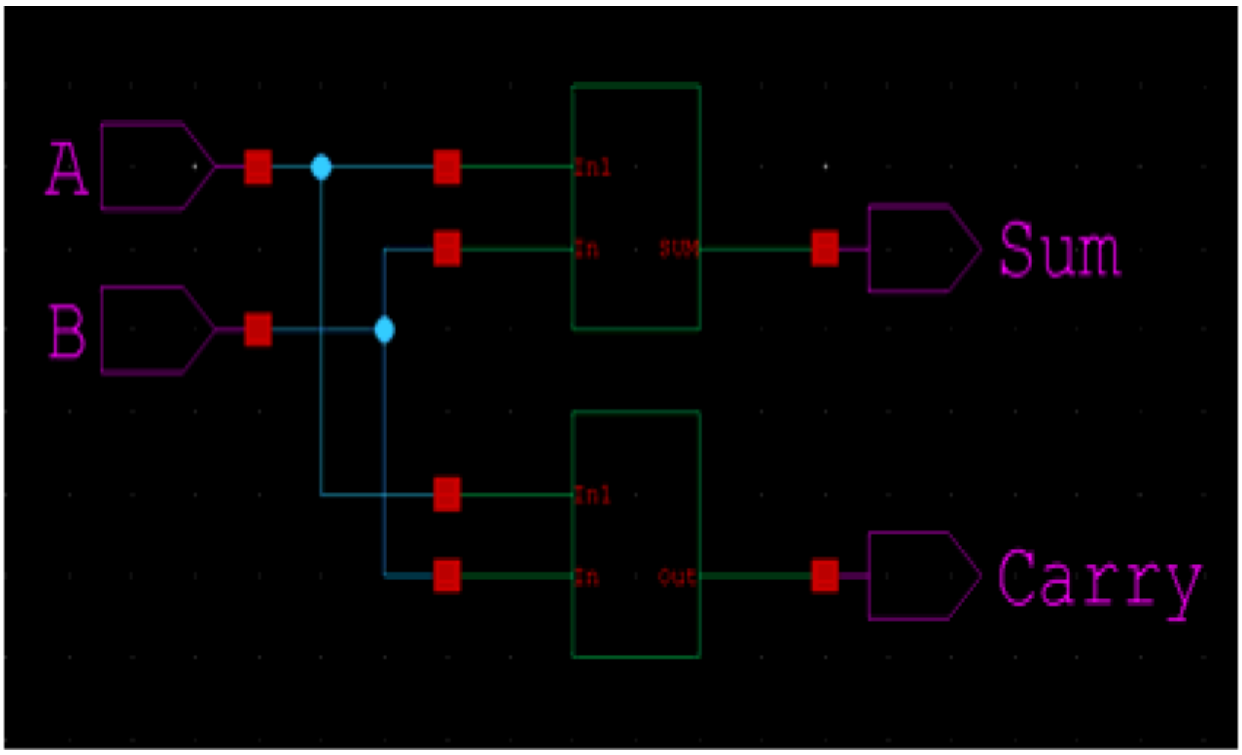
conflicting design criteria are power consumption and speed. Taking into consideration these constraints, the design of low power multiplier is of great interest. As reported in Brent (1982), to get the best power and area requirements of the computational complexities in the VLSI circuits, the length and width of transistors are shrunk into the deep submicron region, handled by process engineering.

In recent years, the literatures have identified several types and designs of adiabatic circuits. For instance, 2N2N2P, PFAL, pass transistor adiabatic logic, clocked adiabatic l Logic, improved pass-gate adiabatic logic, and adiabatic differential switch Logic were designed and achieved considerable energy savings, compared with conventional CMOS design (Choudhary, 2008; Cornelius, 2006; Geer, 2005; Govindarajulu, 2008; Kursun, 2002; Liu, 1994; Lo, 1994). In Lynch (1992), complementary pass transistor adiabatic logic circuit was discussed, in which the nonadiabatic energy loss of output loads has been completely eliminated. In Martin (1992), adiabatic CPL circuits using two-phase power clocks were presented. In Maezawa (1997), energy saving design technique achieved by latched pass transistor with adiabatic logic was presented. Many research methods in the adiabatic logic have been attempted to reduce the power dissipation of VLSI circuits, reported in Lo (1994), Lynch (1992), Martin (1992), Maezawa (1997), Nowick (1996), Rahman (2013), Von (1966).

Many research efforts in the multiplier design have been introduced to obtain energy efficiency in VLSI circuits. A 1.5 ns 32-b CMOS ALU in double pass-transistor logic was proposed to improve the circuit performance at reduced

Figure 1: Adder



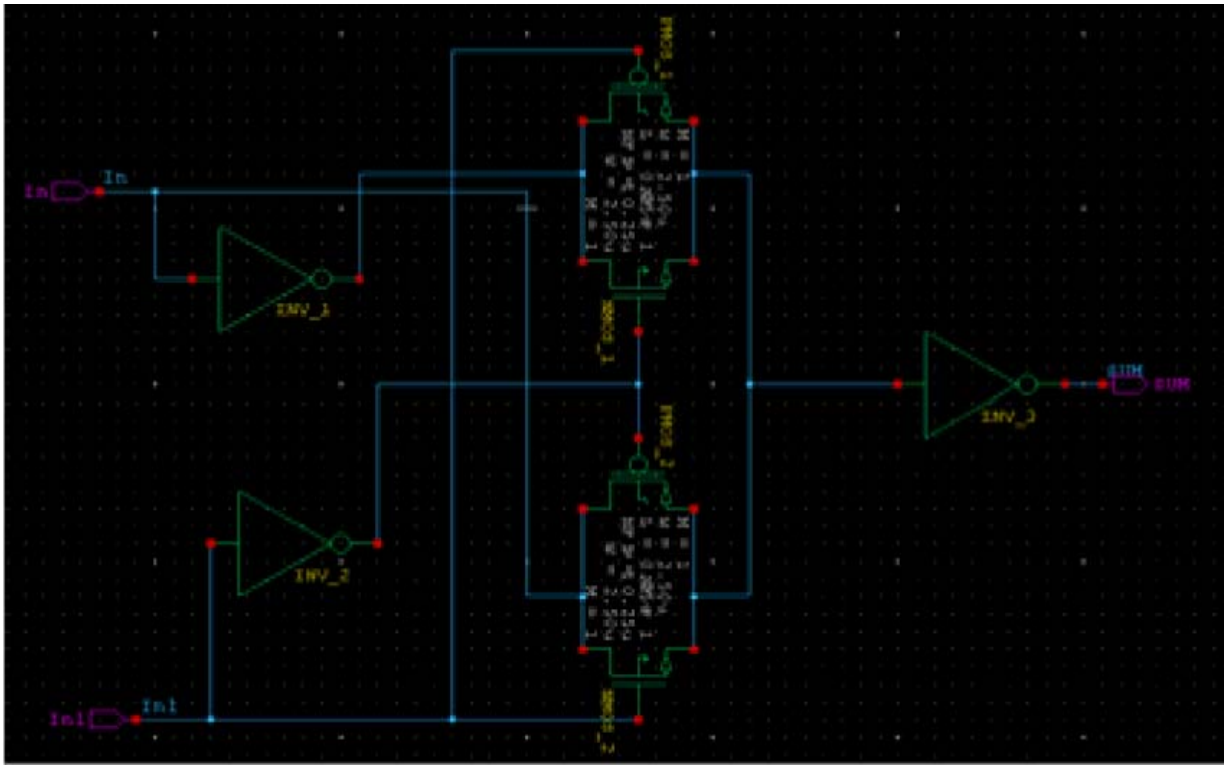
supply voltage ranges. A low power multiplier using 4-2 compressor based on adiabatic CPL circuit is described. By the scaling rules set by Dennard, smart optimization can be achieved by means of timely introduction of new processing techniques in device structures and materials. In Brent (1982), low power multiplier design using complementary pass transistor asynchronous adiabatic logic is investigated, which exhibits low power and reliable logical operations.

ASYNCHRONOUS ADIABATIC LOGIC (AAL)

Asynchronous adiabatic logic is a unique design technique which combines the energy saving benefits of asynchronous logic and adiabatic logic. Like adiabatic circuits, asynchronous circuits are also a promising technology to focus on low power, highly modular digital circuits. One of the properties of asynchronous systems which make them useful in these applications is that circuits include a built-in insensitivity to variations in power supply voltage, with a lower voltage resulting in slower operation rather than the functional failures that would be seen if traditional synchronous systems were used. Another benefit is the fact that when an asynchronous system is idle, it will not utilize clock signals, whereas in synchronous systems, these clock signals are propagated throughout the entire system and convert energy to heat, often without performing any useful computations.

In contrast to the synchronous circuits, asynchronous circuits perform handshaking between their components to perform all

Figure 2: Half Adder



necessary synchronization, communication, and sequencing of operations. Asynchronous circuits fall into different classes, each offering different advantages. The main privilege of this circuit is its low power consumption, stemming from its elimination of clock drivers and the fact that no transistor ever transitions unless it is performing a useful computation.

EXISTING METHOD

The architecture and theory behind Asynchronous Parallel Adder using recursive approach is presented.

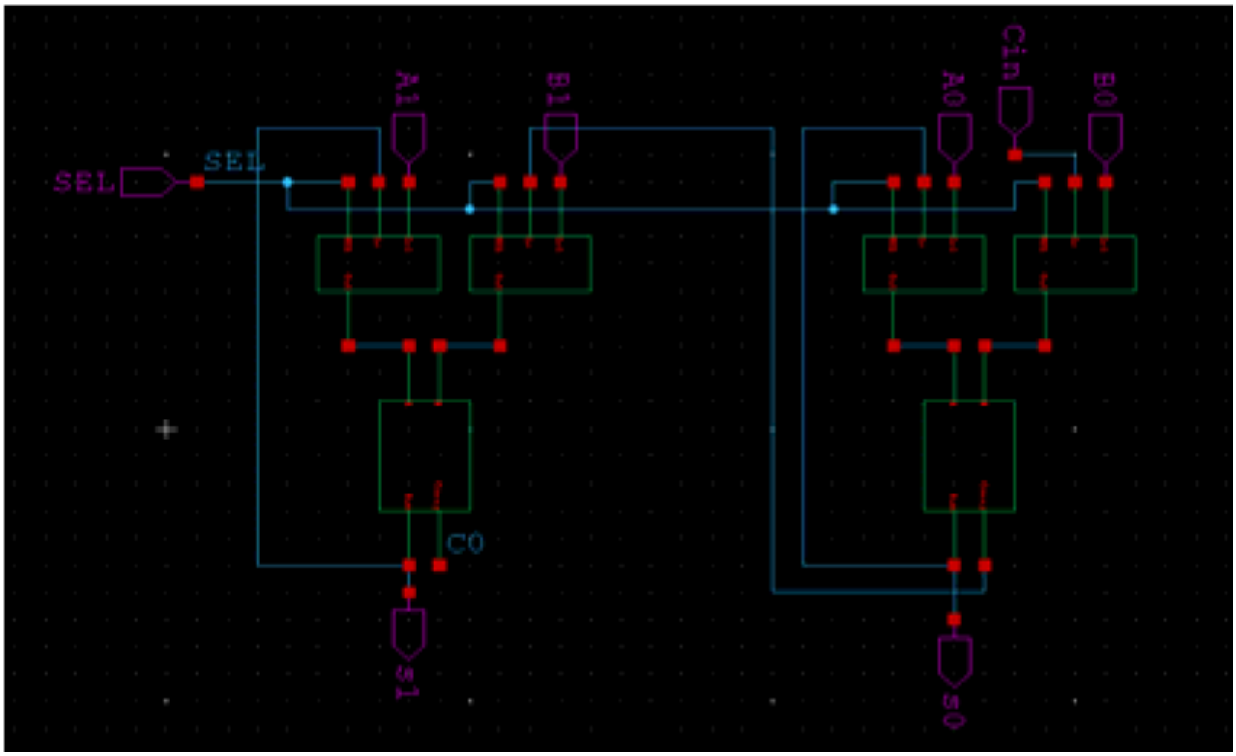
The general architecture of the adder is shown in Figure 1. Req handshake signal is required for the selection input for two-input multiplexers from a single 0 to 1 transition denoted by SEL. During the initial phase SEL = 0, the actual operands are initially selected and will switch to feedback/carry paths for iterative phase using SEL = 1. Multiple recursions occur through the feedback path and continue until all the carry values assume zero values to achieve completion.

The sensor nodes can be communication each other without via base station and the sensor networks application may be one of method or combine two kinds of methods. For example, CAFEE in categorization of the sensor nodes into many clusters, and according to the algorithm select one of clusters head of them. The clusters head will be a management and then the process of the nodes been cluster, then communication between the node and sink. The cluster head is like a base station.

PROPOSED DESIGN

The main objective of this paper is to design low power multiplier with energy efficient full adder cell using double pass transistor with asynchronous

Figure 3: Radix 4 Circuit



adiabatic logic. The logic scheme for full adder cell is illustrated in Figure 1. In this, entire system consists of two main blocks, such as logical block and control and regeneration (C&R) block.

Power Clock

In adiabatic circuits, the supply voltage behaves as the clock of the circuit by providing the power, to the circuit and for this reason, it is called power clock. One of the main concerns in the adiabatic logic circuits is the power clock generation. In these circuits, the supply voltage is desired to be a ramping voltage. In the conventional synchronous adiabatic circuits, rather driving each adiabatic logic unit with an externally supplied clock phase, each block is controlled and powered by control signal generated by the C&R block with the help of the logical output of the previous stage. In the design of VLSI circuits, power clock design is a major issue, because the whole transistor logic system shares the power clock. The power clock switching circuit will also dissipate the most power in the logic. Nowadays multiple phase clocks and clock pipelining are the most followed techniques to reduce power dissipation in the power clocks.

The synchronous clock system utilizes the clock source globally; that is, single clock is shared and restored by the large number of logical gates in parallel. Here switching loss of the power clock generator is more as in the CMOS circuit operation.

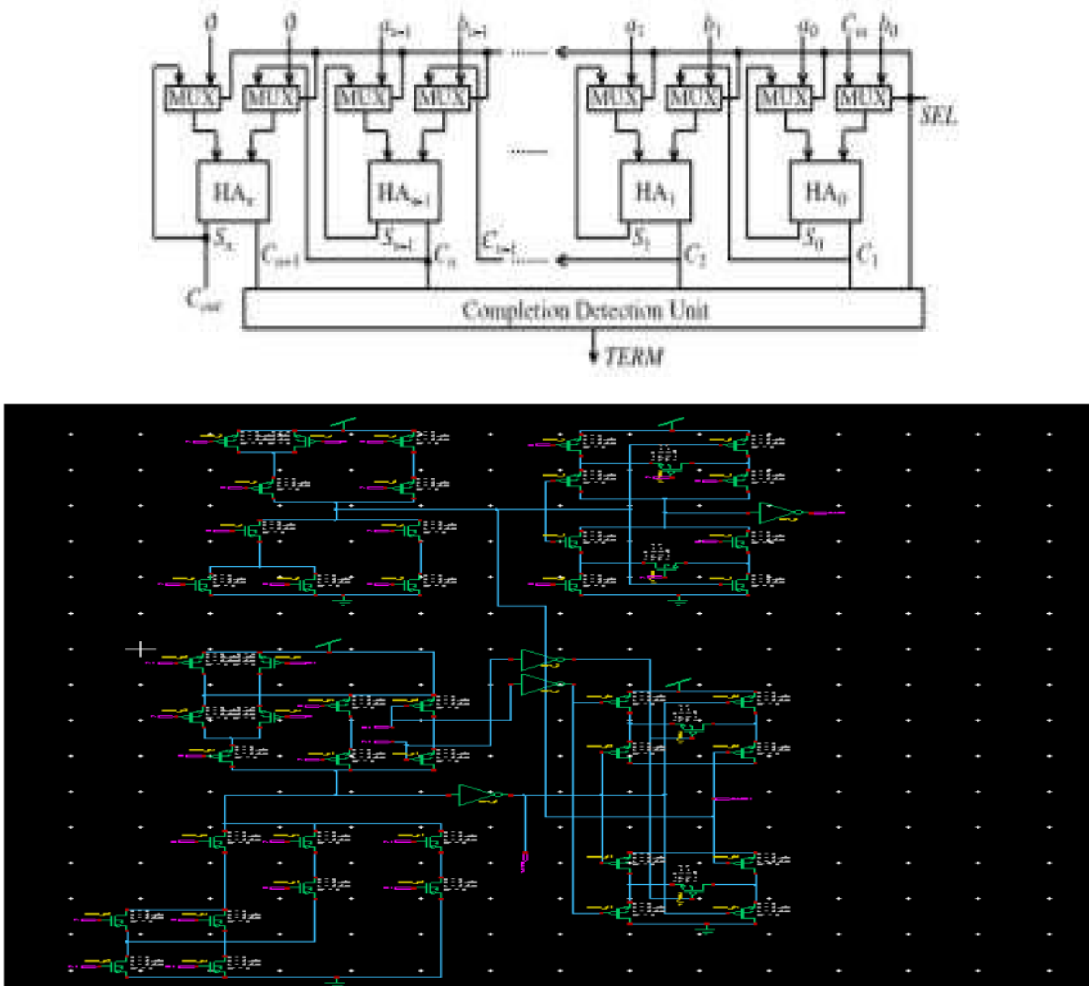
The simple construction of the pass transistor logic makes it easy to adjust the sizing of transistors to get the desired charging and discharging time; hence the slope of the output control signal minimizes the power. The clock energy in the asynchronous clock system is locally stored in the C&R block, and it has been used for later gates; the loss of energy of each operation will be taken from its clock source. The local regeneration stores the intermediate energy. This energy is provided to the required operations for the next level of logic. However, the initial requirement of power from the clock generator remains the same; after powering up the logical sequence, power taken from the power clock is reduced drastically.

The proposed multiplier design scheme is illustrated in Figure 2. In this, data out signal of any full adder is not only going into next full adder as data input. But at the same time, it is used to generate a control signal for the next full adder using C&R block 1. This technique helps to save the required power clock generator with less power.

The proposed approach assumes heterogeneous network with the sensor nodes having different energy levels and processing power. Some high computing nodes are deployed nearby each other. All the nodes with high initial energy level and processing power are selected. Some nodes from the set are selected as Cluster Head (CH) according to their location. Each CH

defines its communication range in terms of power level to form cluster. Some nodes with comparable energy and processing power in the CH range are asked to go to sleep and information about those nodes is maintained with the CH. Each CH sends a hello request message to all the nodes within its communication range to become the cluster member. This process will be repeated for all the CH. All the cluster members will send the sensed data to the CH. The CH will send the aggregated data to the Base Station directly or by using some Intermediate CH.

Figure 4: Radix Full Adder Circuit



The purpose of this protocol subjects are shielded from all time cues, often by a constant light protocol, by a constant dark protocol or by the use of light/dark conditions to which the organism cannot entrain such as the ultra short protocol of one hour dark and two hours light plays a vital role in communication and computer network in which program models the behaviour of a network by calculating the interaction between the different network entities using mathematical formulas. The behaviour of the network can be observed in a test lab.

EXPERIMENTAL RESULTS

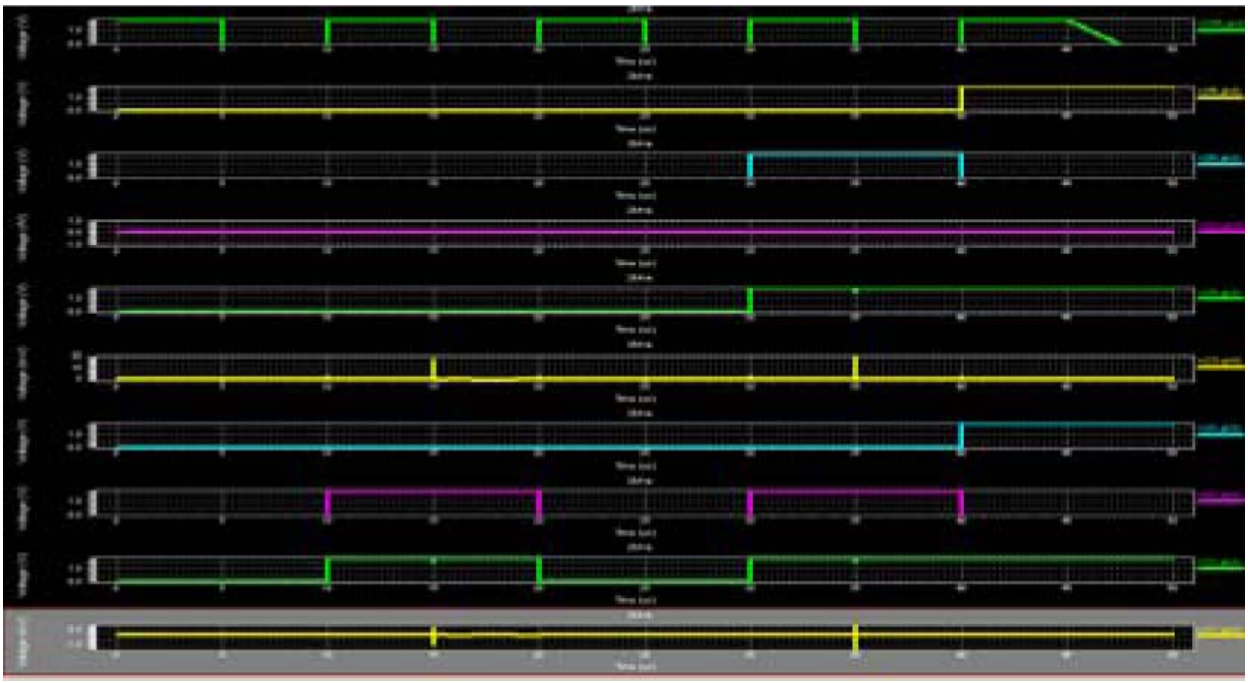
Existing Model

Simulations results Simulation output is to be obtained by using CADENCE in digital design environment. The adder was designed using multiplication technique. In this method usage the area, power consumption and time are obtained

GRAPH OUTPUT

Figure 4 shows the simulation results of parallel prefix adder. It represents 8 bit hexadecimal values henceclock is not assigned. The timing is

Figure 5: Radix 4 Bit Output

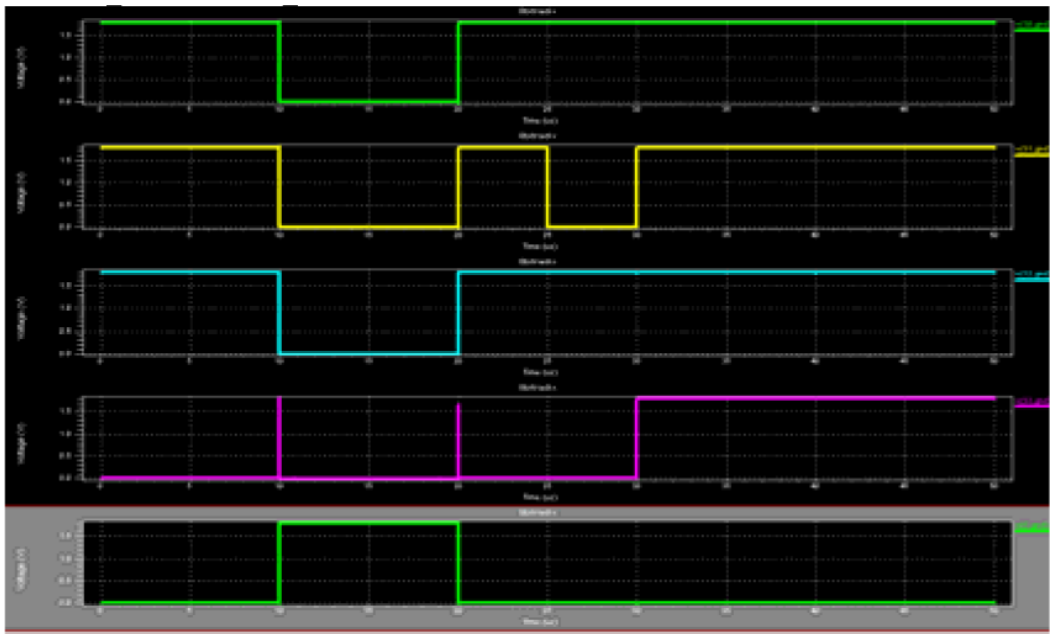


varied for simulation the carry and propagate values are described for each input and output values are assigned using the force operation the run time is varied for each simulation.

Graph Output

The Figure 1 denotes the energy diagram of existing system. In this system the threshold value

Figure 6: Radix 8 Bit Output



only fixed to the node operation. The source node and destination nodes are automatically considered. For this node threshold value decreases the packet losses will be created.

PROPOSED METHOD

Basic Radix-2FA

The main approach in this work is to reduce the PDP and EDP of an adder and to reduce the delay due to carry propagation. We use the 24-transistor mirror FA as a base for our design, which is illustrated in Figure 3. To optimize the speed, we joined two FAs in a single block and use the carry look-ahead technique to shorten the carry path within the radix-2FA block. The transistor schematic is shown in Figure 3. The total transistor count is 56. Boolean equations for the two carry and two sum gates of the carry-accelerated design are given below.

The circuit for computing the least significant sum bit *S*0 is the same as that of a radix-2 FA. We use the carry look ahead technique to design the circuitry for the most significant carry bit *C*out. Equation (5) is similar to the equation for a CLA with the difference that generate and propagate signals are generated explicitly for the CLA. To implement the function that computes the most significant sum bit *S*1 with a single gate, we invert the inputs *A*1, B1 and *C*1.

SIMULATION GRAPH

For the simulation process the threshold value, Source node, Destination node and load node has been created. For the simulation process the source node has been to deliver the data between packet delivery ratios. In order to the process the load node has varied by means of threshold value. The data has delivered by clusters by means of load node.

Figure 7: Radix 16 Bit Output

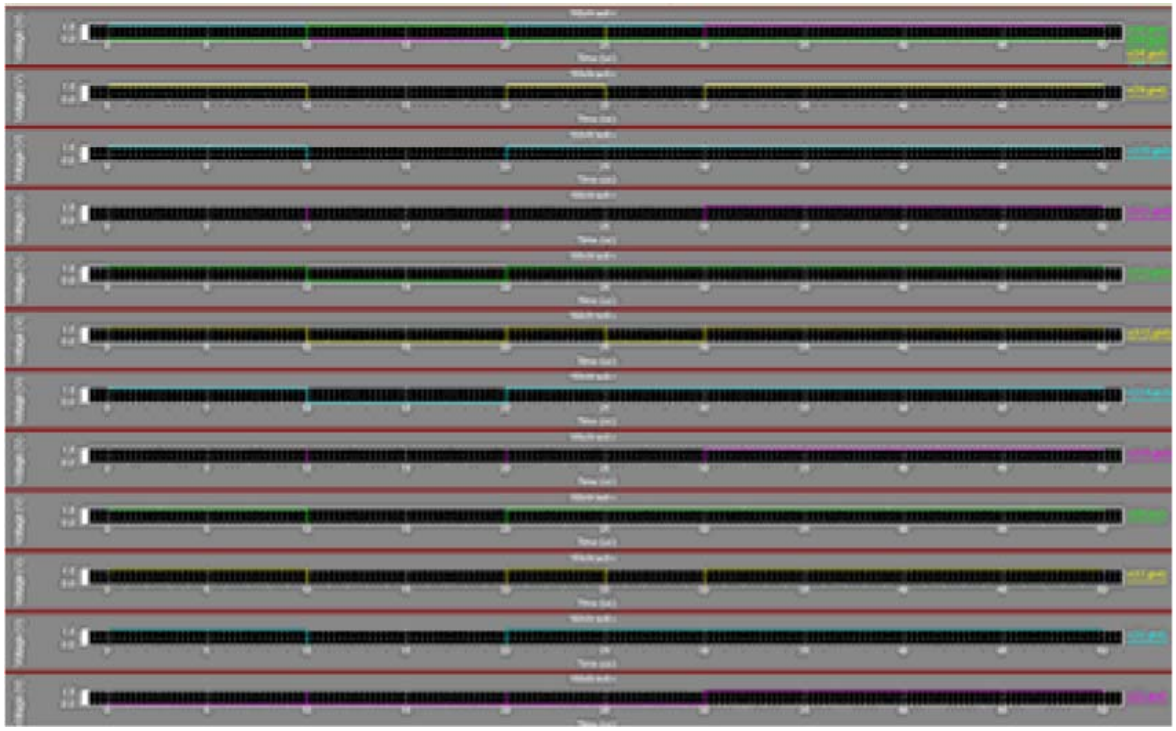
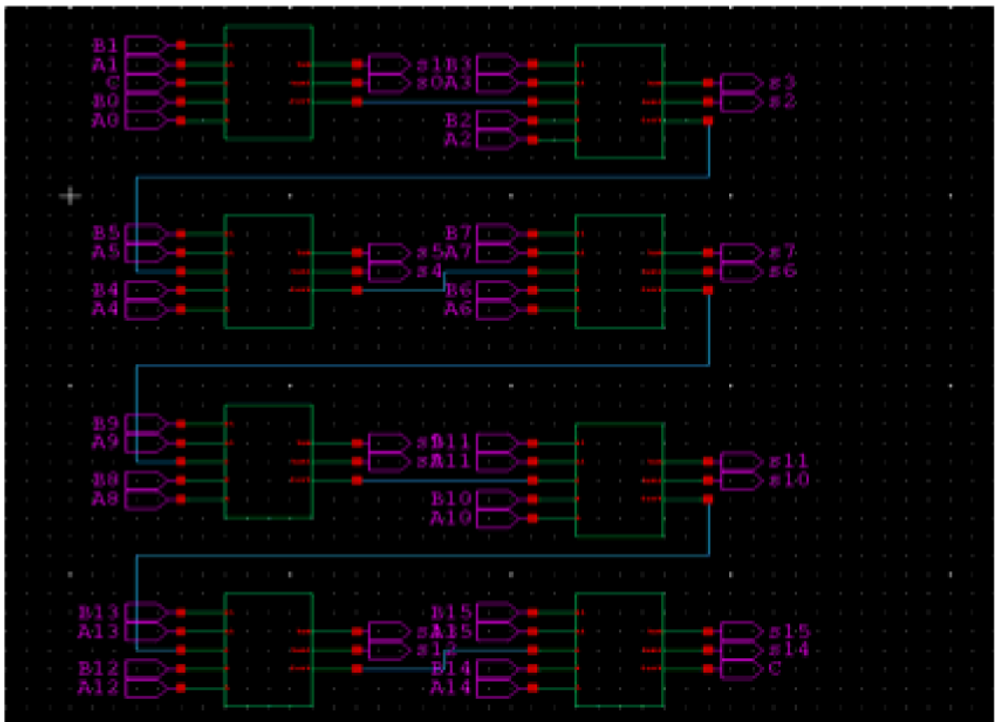


Figure 8: Radix 16 Circuit



The above graph mentioned to that the energy of an the source and destination. The value has been constant in order to using the Load node, it named as alternate node. This method has processed to been the packet delivery ratio.

This method has processed to been Energy value of the Destination node, because of that alternate node has been changed to that value of threshold voltage.

CONCLUSION

A parallel prefix adder design is proposed for overall power consumption. The proposed adder provides overall area and power than the previous methods. The parallel asynchronous self timed adder circuit is efficiently described using a handshaking protocol and also compared with other adders proposed adders. The MAC unit is implemented and the process is achieved efficiently. Simulation results demonstrate the effectiveness of the proposed framework in parallel prefix adder using multiplication through addition process. The proposed method is implemented using digital TANNER environment

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