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Research Paper

HIGH SPEED COMPARATOR ARCHITECTURE FOR FAST BINARY COMPARISON

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This paper provides an experience of new comparator model gives large range, with faster operation by converting n-bit CMOS cells. This comparator make use of novel scalable parallel prefix constructs strategic advantage by comparing Most Significant Bit (MSB) outcomes which is scheduled bit wise towards the Least Significant Bit (LSB). Comparing as the bits are equal and the obtained result is used for decision module we presented an n bit high-speed low-power comparator using regular digital hardware structures consisting of two modules which are comparison resolution module and decision module. The structured modules are parallel prefix trees with repeated cells in the form of simple stages. The design is simulated and synthesized in the XILINX ISE EDA tool using the verilog language.

Keywords: Comparator, Parallel architecture, Compares look ahead logic

INTRODUCTION

A digital comparator or magnitude comparator is a hardware electronic device that takes two numbers as input in binary form and determines whether one number is greater than, less than or equal to the other number. Comparators are used in a Central Processing Units (CPU) and microcontrollers. Examples of digital comparator include the CMOS 4063 and 4585 and the TTL 7485 and 74682-'89. The analog equivalent of digital comparator is the voltage comparator. Many microcontrollers have analog comparators on some of their inputs that can be read or trigger an interrupt.This is useful if we want to compare two variables and want to produce an output when any of the above three conditions are achieved. For example, produce an output from a counter when a certain count number is reached. Consider the simple 1-bit comparator below.

We may notice two distinct features about the comparator from the above truth table. Firstly, the circuit does not distinguish between either two "0" or two "1"'s as an output A = B is produced when they are both equal, either A = B = "0" or A = B = "1". Secondly, the output condition for A = B resembles that of a commonly available logic gate, the Exclusive-NOR or Ex-NOR function (equivalence) on each of the n-bits giving: $Q = A \oplus B$

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Figure 1: 1-bit Comparator

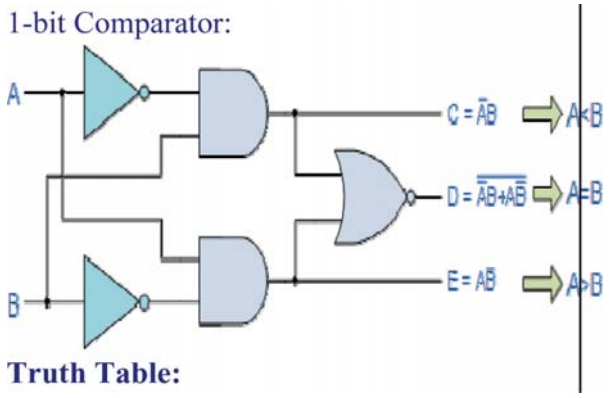


Table 1: Truth Table of Comparator

Inputs		Outputs		
B	A	A > B	A = B	A < B
0	0	0	1	0
0	1	1	0	0
1	0	0	0	1
1	1	0	1	0

Digital comparators actually use Exclusive-NOR gates within their design for comparing their respective pairs of bits. When we are comparing two binary or BCD values or variables against each other, we are comparing the "magnitude" of these values, a logic "0" against a logic "1" which is where the term Magnitude Comparator comes from as well as comparing individual bits, we can design larger bit comparators by cascading together n of these and produce a n-bit comparator just as we did for the n-bit adder in the previous tutorial. Multi-bit comparators can be constructed to compare whole binary or BCD words to produce an output if one word is larger, equal to or less than the other. A very good example of this is the 4-bit Magnitude Comparator. Here, two 4-bit words ("nibbles") are compared to each other to produce the relevant output with one word connected to inputs A and the other to be compared against connected to input B.

COMPARATOR ANALYSIS

In electronics, a **comparator** is a device that compares two voltages or currents and outputs a digital signal indicating which is larger. It has two analog input terminals V_+ and V_- and one binary digital output V_o. The output is ideally

$$V_0 = \begin{cases} 1, & if\ V_+ > V_- \\ 0, & if\ V_+ < V_- \end{cases}$$

A comparator consists of a specialized high-gain differential amplifier. They are commonly used in devices that measure and digitize analog signals, such as Analog-to-Digital Converters (ADCs), as well as relaxation oscillators.

DIFFERENTIAL AMPLIFIER

The differential voltages must stay within the limits specified by the manufacturer. Early integrated comparators, like the LM111 family, and certain high-speed comparators like the LM119 family, require differential voltage ranges substantially lower than the power supply voltages (±15 V vs. 36 V). *Rail-to-rail* comparators allow any differential voltages within the power supply range. When powered from a bipolar (dual rail) supply,

$$V_{S-} \leq V_+, V_- \leq V_{S+}$$

or, when powered from a unipolar TTL/CMOS power supply:

$$0 \leq V_+, V_- \leq V_{cc}$$

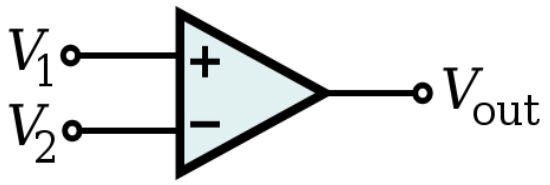
Specific rail-to-rail comparators with p-n-

p input transistors, like the LM139 family, allow input potential to drop 0.3 V below the negative supply rail, but do not allow it to rise above the positive rail. Specific ultra-fast comparators, like the LMH7322, allow input signal to swing below the negative rail and above the positive rail, although by a narrow margin of only 0.2 V. Differential input voltage (the voltage between two inputs) of a modern rail-to-rail comparator is usually limited only by the full swing of power supply.

OP-AMP VOLTAGE COMPARATOR

An operational amplifier (op-amp) has a well balanced difference input and a very high gain. This parallels the characteristics of comparators and can be substituted in applications with low-performance requirements.

Figure 2: A Simple op-amp Comparator



In theory, a standard op-amp operating in open-loop configuration (without negative feedback) may be used as a low-performance comparator. When the non-inverting input (V+) is at a higher voltage than the inverting input (V-), the high gain of the op-amp causes the output to saturate at the highest positive voltage it can output. When the non-inverting input (V+) drops below the inverting input (V-), the output saturates at the most negative voltage it can output. The op-amp's output voltage is limited by the supply voltage. An op-amp operating in a linear mode with negative feedback, using a balanced, split-voltage power supply, (powered by ± VS) has its transfer function typically written as:

$$V_{out} = A_o(V_1 - V_2).$$

However, this equation may not be applicable to a comparator circuit which is non-linear and operates open-loop (no negative feedback).

In practice, using an operational amplifier as a comparator presents several disadvantages as compared to using a dedicated comparator:

1. Op-amps are designed to operate in the linear mode with negative feedback. Hence, an op-amp typically has a lengthy recovery time from saturation. Almost all op-amps have an internal compensation capacitor which imposes slew rate limitations for high frequency signals. Consequently an op-amp makes a sloppy comparator with propagation delays that can be as slow as tens of microseconds.
2. Since op-amps do not have any internal hysteresis, an external hysteresis network is always necessary for slow moving input signals.
3. The quiescent current specification of an op-amp is valid only when the feedback is active. Some op-amps show an increased quiescent current when the inputs are not equal.
4. A comparator is designed to produce well limited output voltages that easily interface with digital logic. Compatibility with digital logic must be verified while using an op-amp as a comparator.
5. Some multiple-section op-amps may exhibit extreme channel-channel interaction when used as comparators.
6. Many op-amps have back to back diodes between their inputs. Op-amp inputs usually

follow each other so this is fine. But comparator inputs are not usually the same. The diodes can cause unexpected current through inputs.

A dedicated voltage comparator will generally be faster than a general-purpose operational amplifier pressed into service as a comparator. A dedicated voltage comparator may also contain additional features such as an accurate, internal voltage reference, an adjustable hysteresis and a clock gated input. A dedicated voltage comparator chip such as LM339 is designed to interface with a digital logic interface (to a TTL or a CMOS). The output is a binary state often used to interface real world signals to digital circuitry (see analog to digital converter). If there is a fixed voltage source from, for example, a DC adjustable device in the signal path, a comparator is just the equivalent of a cascade of amplifiers. When the voltages are nearly equal, the output voltage will not fall into one of the logic levels, thus analog signals will enter the digital domain with unpredictable results. To make this range as small as possible, the amplifier cascade is high gain. The circuit consists of mainly Bipolar transistors. For very high frequencies, the input impedance of the stages is low. This reduces the saturation of the slow, large P-N junction bipolar transistors that would otherwise lead to long recovery times. Fast small Schottky diodes, like those found in binary logic designs, improve the performance significantly though the performance still lags that of circuits with amplifiers using analog signals. Slew rate has no meaning for these devices. For applications in flash ADCs the distributed signal across eight ports matches the voltage and current gain after each amplifier, and resistors then behave as level-shifters. The LM339 accomplishes this with an open collector output. When the inverting input is at a higher voltage than the non inverting input, the output of the comparator connects to the negative power supply. When the non inverting input is higher than the inverting input, the output is 'floating' (has a very high impedance to ground). Gain of op amp as comparator is get from this equation

V(out)=V(in)*A

With a pull-up resistor and a 0 to +5 V power supply, the output takes on the voltages 0 or +5 and can interface with TTL logic:

$V_+ \geq V_-$ when else 0.

REAL TIME APPLICATIONS

Null Detector

A null detector is one that functions to identify when a given value is zero. Comparators can be a type of amplifier distinctively for null comparison measurements. It is the equivalent to a very high gain amplifier with well-balanced inputs and controlled output limits. The circuit compares the two input voltages, determining the larger. The inputs are an unknown voltage and a reference voltage, usually referred to as vu and vr. A reference voltage is generally on the non-inverting input (+), while vu is usually on the inverting input (-). (A circuit diagram would display the inputs according to their sign with respect to the output when a particular input is greater than the other). The output is either positive or negative, for example +/-12 V. In this case, the idea is to detect when there is no difference between in the input voltages. This gives the identity of the unknown voltage since the reference voltage is known.

When using a comparator as a null detector, there are limits as to the accuracy of the zero value measurable. Zero output is given when the magnitude of the difference in the voltages multiplied by the gain of the amplifier is less than

the voltage limits. For example, if the gain of the amplifier is 106, and the voltage limits are +/-6 V, then no output will be given if the difference in the voltages is less than 6 ìV. One could refer to this as a sort of uncertainty in the measurement.

Zero Crossing Detector

For this type of detector, a comparator detects each time an ac pulse changes polarity. The output of the comparator changes state each time the pulse changes its polarity, that is, the output is HI (high) for a positive pulse and LO (low) for a negative pulse squares the input signal.

Relaxation Oscillator

A comparator can be used to build a relaxation oscillator. It uses both positive and negative feedback. The positive feedback is a Schmitt trigger configuration. Alone, the trigger is a bi stable multi vibrator. However, the slow negative feedback added to the trigger by the RC circuit causes the circuit to oscillate automatically. That is, the addition of the RC circuit turns the hysteretic bi stable multi vibrator into an astable multi vibrator.

Level Shifter

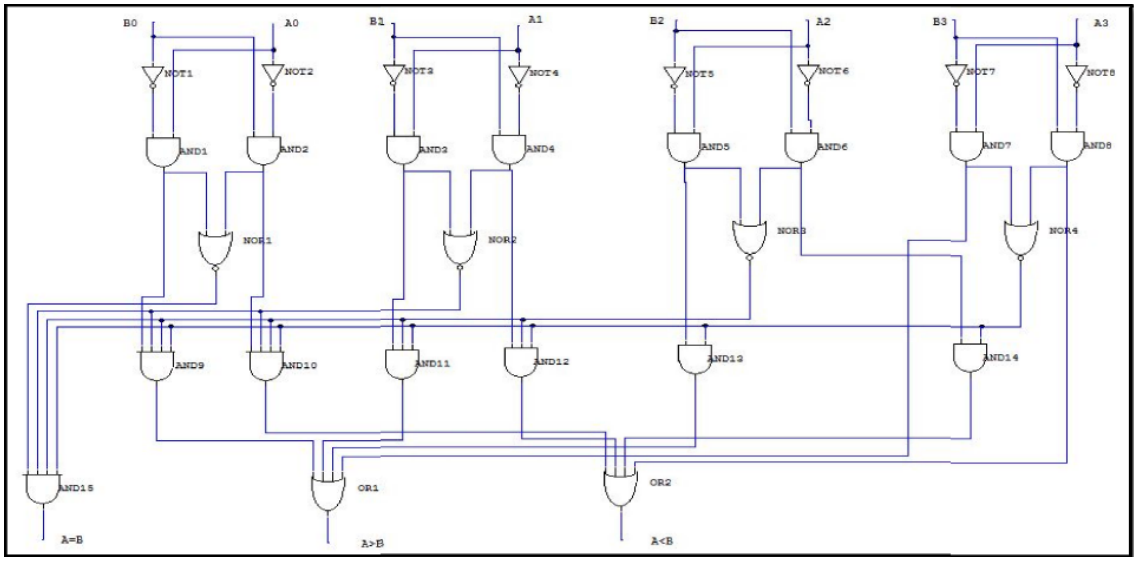
This circuit requires only a single comparator with an open-drain output as in the LM393, TLV3011 or MAX9028. The circuit provides great flexibility in choosing the voltages to be translated by using a suitable pull up voltage. It also allows the translation of bipolar ±5 V logic to unipolar 3V logic by using a comparator like the MAX972.

Analog-to-Digital Converters

When a comparator performs the function of telling if an input voltage is above or below a given threshold, it is essentially performing a 1-bit quantization. This function is used in nearly all analog to digital converters (such as flash, pipeline, successive approximation, delta-sigma modulation, folding, interpolating, dual-slope and others) in combination with other devices to achieve a multi-bit quantization.

To compare two sets of digital data in order to determine if they are 100% identical. Binary compares are commonly done and are the only guarantee that two files are the same, bit for bit. One could read the contents of two word

Figure 3: Comparator Architecture



processing documents side-by-side, and the words and sentences could be the same, but the file formats could be different. A binary compare of the two files would determine if they were absolutely identical in structure.

Traditional magnitude comparator is shown in Figure. The design is a parallel architecture. The circuit has three output bits: A>B, A<B, A=B. In many applications, only two output signals A>B, A<B are sufficient. The output bit (A=B) goes high if all the bits of A are equal to the corresponding bits of B. The two output signals A>B and A<B, are determined based on the following two conditions.

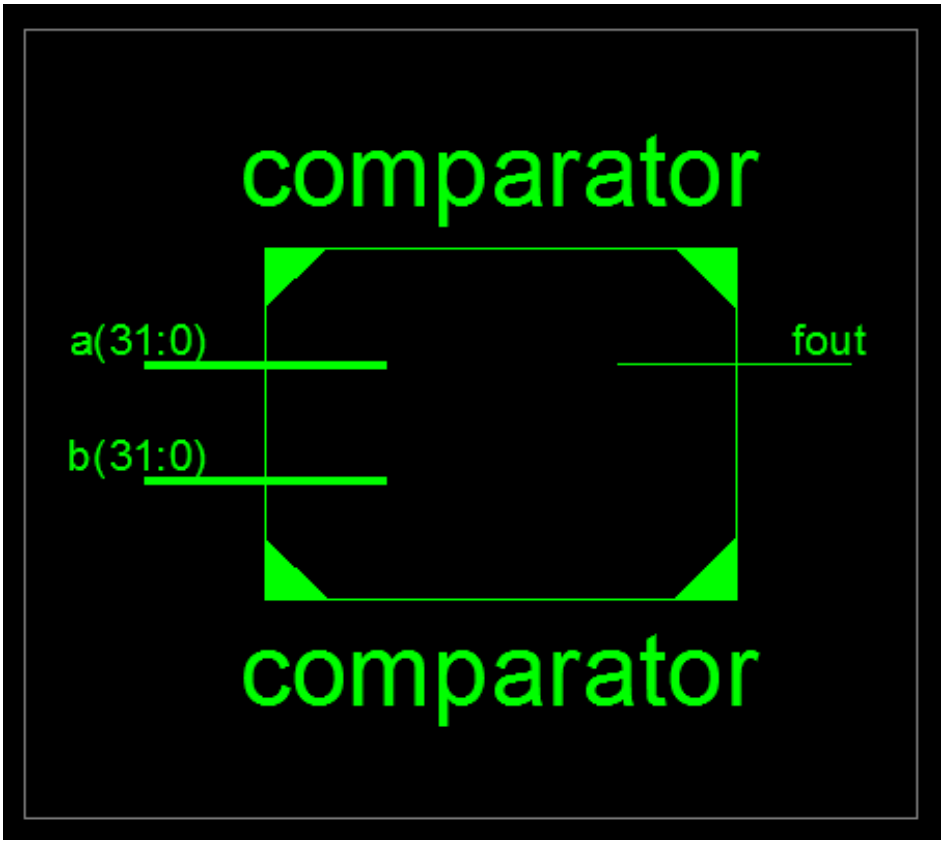
- If MSBs of the two numbers are unequal, i.e., when Ai=1, Bi =0 then A>B or Ai=0, Bi =1 for A<B.
- OR if the pair of bits in the significant bit positions are equal, and LSBs are different, i.e., Ai=Bi and Ai-1= 1, Bi-1 =0 then A>B or Ai=Bi and Ai-1=0, Bi-1=1

  then A<B.

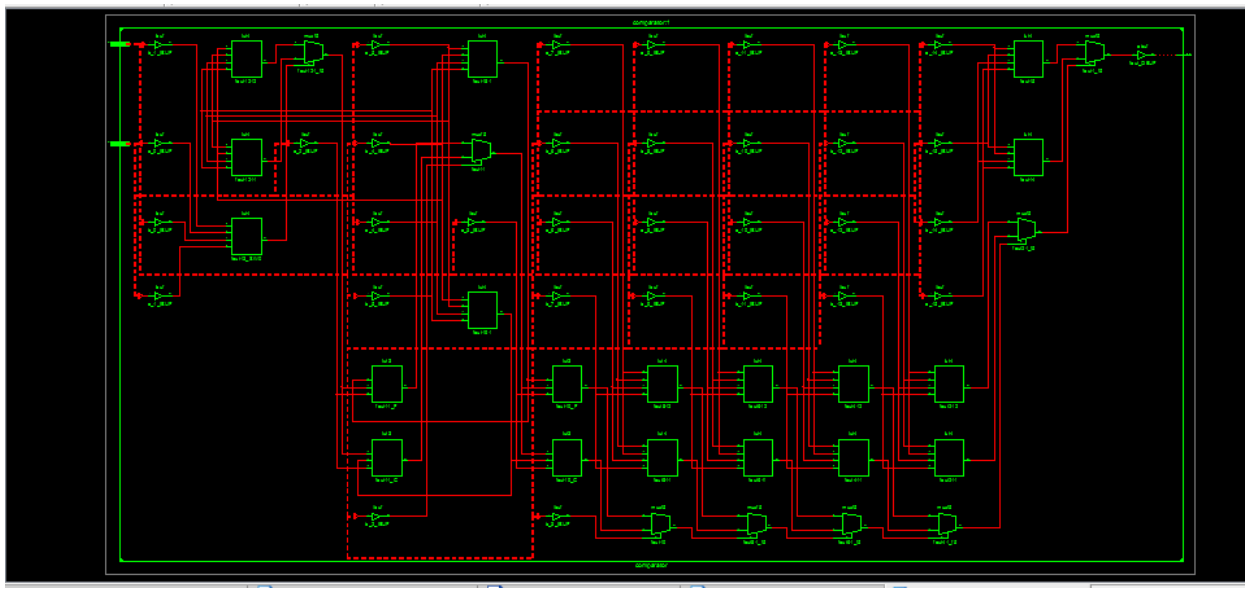
RESULTS

In this paper we design a comparator which make use of novel scalable parallel prefix constructs strategic advantage by comparing Most Significant Bit (MSB) outcomes which is scheduled bit wise towards the Least Significant Bit (LSB).The inputs to the comparator are A and B of 32 bit width and fout of single bit width. For example if a = 45, and b = 30, the output = 1.The output fout will be 1 if and only if a is greater than b.

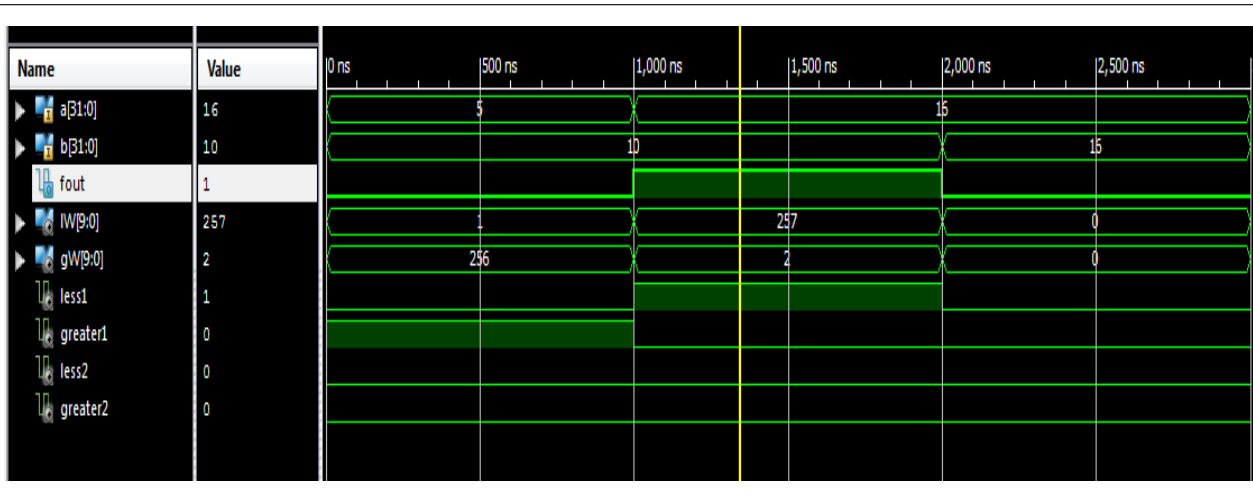
RTL Schematic View



Technology Schematic View



Waveform



CONCLUSION

The proposed comparators have been discussed, simulated and compared with the traditional one. Simulation results decrease in path delay in case of the proposed architecture-I and decrease in path delay in case of proposed architecture-II over traditional architecture. In our proposed design, we have extended our design to 32 bits with efficient path delay. In future, the comparator bit size can increased to 128 considering the fear factors like delay and power as a important factors, which should not be increased so that it can affect the performance of the comparator. Future work will include additional circuit optimizations to further reduce the power dissipation by adapting dynamic and analog implementations for the comparator resolution module and a high-speed zero-detector circuit for the decision module. Given that our comparator is composed of two balanced timing modules, the structure can be divided into two or

more pipeline stages with balanced delays, based on a set structure, to effectively increase the comparison throughput.

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