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Research Paper

REDUCTION OF LEAKAGE CURRENT IN SIX STAGE CHARGE PUMP USING STACKING POWER GATING TECHNOLOGY

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CMOS is used to construct the integrated circuits with a low level of static leakage. With this low-level leakage, we are designing all the transistor circuits in CMOS logic. To control this static leakage in the circuits, the supply voltage is a major concern. Here the step-up converters with charge pump and the level for maintaining its threshold voltage (VT) are to be analyzed and proposed. Here we are going to propose the novel approach as body bias effect and sub-threshold logic. This will be applied to the step-up converters for energy harvesting applications. The backward control is to be processed for control the internal voltage when the charge transfer switch could be in activation. When the supply voltage is to be raised from the fixed voltage level, it will be the turn OFF the transistor. The maximum level of the converters circuits contains the branch A and branch B which could be contained all p-MOS and n-MOS combinations. The oscillator circuit also designed and applied to the proposed six stage charge pump circuit to reduce the power consumption. To reduce the standby mode leakage, we are designing the circuit by using power gating logic. These circuits are to be designed and verified by using the TANNER T-SPICE TOOLS.

Keywords: Low power, Charge pump, Body bias, Power gating

INTRODUCTION

A charge pump circuit provides a voltage or a voltage of reverse polarity to upgrade the amplification process. In several applications like Power IC, continuous-time filters, and EEPROM, voltages on top of the facility providers square measure often times needed. Redoubled voltage levels square measure obtained from a charge pump as the results of transferring charges to an electrical phenomenon load and do not involve amplifiers or transformers.

For that reason, a charge pump may be a device of alternative in semiconductor technology wherever traditional vary of operative voltages is prescribed. Charge pumps usually operate at high-frequency level so as to extend their output power among an inexpensive size of total capacitance used for charge transfer. This

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operative frequency is also adjusted by compensating for changes in the power needs and saving the energy delivered to the charge pump.

From dozens of millivolts, but it needs external high voltage sources or expensive mechanical active devices to start up the system, which limits their practical application. So that only we are modified in that by means of stacking power gating. Apparently, a better approach will build an integrated startup charge pump with stacking power gating, which can generate a high-voltage pulse to bootstrap a step-up converter from a low voltage input.

In this paper, a power gating of startup charge pump is proposed for low voltage and low power operation. The charge pump with an integrated ring oscillator utilizes sub-threshold operation and body bias technique used to enable startup and operate under a low voltage supply. The charge pump is the first utilized both backward control scheme and two branches of Charge Transfer Switches (CTSs) to direct charge flow. The backward control scheme uses the internal boosted voltage for dynamically control the CTS's gate, and the two branches utilize both NMOS and PMOS to implement their switching structure. With a special structure of stacking power gating in CMOS, startup charge pump obtains performance improvement in some of the key specifications. A startup charge pump only works during the startup period of a step-up converter, and it supports a capacitive load.

The rest of this paper is organized as follows. Section II surveys all of the previous works with CMOS startup charge pump in step up converters. Section III describes the concepts of stacking power gating. In Section IV describes the proposed system stacking power gating with startup charge pump. In section V, simulation output waveforms are shown and the comparisons of previous charge pumps are tabulated.

The proposed stacking power gating with charge pump offers best performance at a minimum supply voltage, pumping efficiency, charge transferability and capacitance drivability.

CMOS STARTUP CHARGE PUMP BASED ON BODY BIASING

The startup low voltage six-stage two branch charge pump is designed for low voltage power supply applications was implemented with two CTSs branches and compensated structure in each stage. Two compensated branches are used to transfer charge significantly improves pumping efficiency and reduce output ripples because two pumping branches can provide better charge transferability. In very large devices, there is no need for designing the CTSs, which can lower the effect of the device size on the threshold voltage. Meanwhile, the redistribution loss between the last stage and the output capacitor can be reduced since one of the two branches always provide current to keep the output voltage stable.

A charge pump was designed for low voltage power supply applications; the beginning is to build a ring oscillator which can generate out of phase clock signals. The oscillator must able to work under a voltage supply of several hundred millivolts. It should have a rail-to-rail output swing and the output current drivability should be large. The five stage sub-threshold ring oscillator, the body bias ring oscillator with two buffer stages

are used to operate the inverter in a sub-threshold region. Two phase shifting circuits with large size buffers are used to improve the clock output swing and the current drivability because the clock generator has to drive a total pumping capacitance. A Six stage two branch charge pump.

The input startup voltage of the proposed charge pump circuit is 320 mv, it consists of 6 stages each stage having both upward and downward capacitor. Figure 1(a) and (b) shows the circuit diagram and waveform representation of proposed six stage two branch charge pump.

The charge pump circuit has to be design in the environment of short circuit current limit and the as well as the temperature protection. This could be used for the further processing of the voltage level of conversion from the circuit based on all level of conversion of power and the current limit. This is mainly focused on the power grid applications. In existing system, there are many charge pump has been designed and having many limitations.

In Dickson charge pump the respective switches could be given into the circuit that is the possible combination of the n-MOS and the p-MOS. This could be switches as per the number of stages provided in the circuit combination of the charge pump. From the capacitance for charging and discharging units could be considered. In this charge pump circuit the extension could not be possible and cannot be added to the real-time process. This could cause various errors during the testing of chips.

The proposed charge pump has the highest charge transferability, the largest capacitance drivability and the highest pumping efficiency in this process, a smaller threshold voltage can be achieved by reducing the width-to-length ratio of the device.

Advantages of the six stages two branch charge pump is in given as,

1. The last stage of the two branches is modified more effectively the CTSs should be the turn on/off under low voltage supply.
2. In a standard CMOS process, the two out of phase clock signals are generated under a low voltage supply.
3. Two compensated branches to transfer charge significantly, improve the pumping efficiency and reduce output ripples.

Figure 1a: Charge Pump Based on body biasing

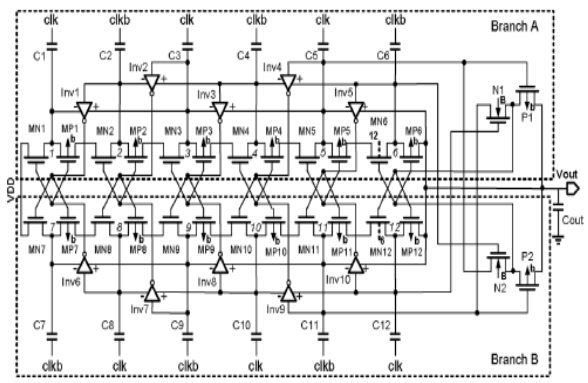
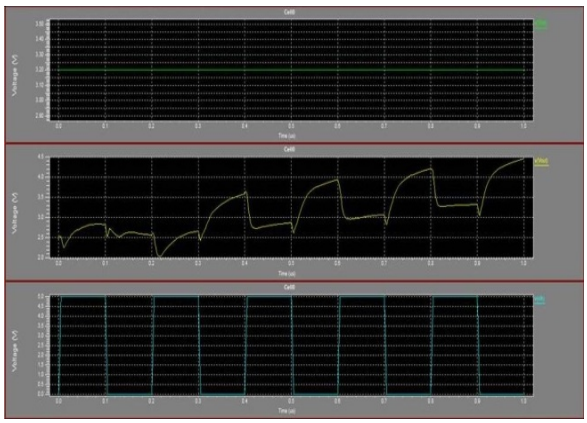


Figure 1b: Corresponding Waveforms

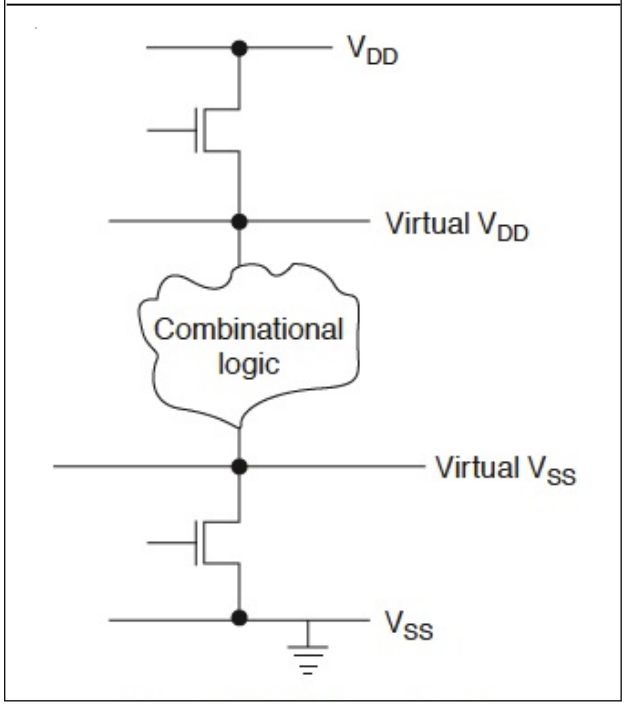


STACKING POWER GATING TECHNIQUE

Power gating is a technique used in integrated circuit design to reduce power consumption, by shutting off the current to blocks of the circuit that are not in use. Internal stacking power gating is more suitable to shut off the block for small intervals of time. Power can be controlled by stacking power gating controllers andto provide power to the circuitry CMOS switches are used. The power gatedoutputs block discharges slowly. Hence voltage levels of the output block spend more time in threshold voltage level (Vth), so it leads to larger short circuit current in the circuit.

Low-leakage PMOS transistors are used as header switches to shut off power supplies, the stacking Power Gating parts of a design in the mode of sleep or standby. NMOS footer switches can also be used as sleep transistors in the design of stacking power gating technique. The sleep transistors can be inserting to splits the chip's power network into a permanent power network connected to the power supply and a virtual power network that drives the cells and can be turned off. By using of a cell- or cluster-based (or fine grain) approaches or a distributed coarse-grained approaches stacking Power Gating can be implemented.

Figure 2: Stacking Power Gating Technique



Power gating technique is widely used to significantly suppress the leakage currents in standby mode. Stacking sleep transistorsare used in stacking power gating technique to reduce the magnitude of peak current and voltage glitches in power rails (i.e) ground bounce noise (Po Hung, 2011). In the proposed power gating technique, if stacking power gating scheme works on two strategies. (1) Reduction of leakage current by stacking effect, (2) Reductions of ground bounce noise by controlling the intermediate node voltage. In the technique stacking effect is used to reduce the leakage current.

PROPOSED SYSTEM

The stacking power gating scheme is the most efficient way for reducing leakage power in standby mode. In this process, we are using large transistors called sleep transistors, in series with the pull-up and pull-down stacks to cut-off the power supply rail from the circuit whenthe circuit is in standby mode. Ground bounce noise is an important issue in the design of nanometer circuits and this inductive noise is also associated with clock gating. Previous work we are design six stage two branch charge pump circuit in startup voltage but it consumes more power. This proposed charge pump has advantages of the low power consumption based on body biasing bulk connection from the each node of operation. And also this charge pump circuit has been

enabled for the lower input voltage (in millivolts) having the bulk output voltages from the clock pulses. The enabling signals that carry the circuit levelof operation from the amplitude degradation of the unit supply to the needed positive up gradation from the input amplitude. This phase difference from the clock pulses into the bulk connection from the unit supply that can be varied as per the input signal. The charge pump with stacking power gating shown Figure 2.

SIMULATION OUTPUT RESULTS

To achieve long-term leakage stacking power reduction is an externally switched power supply is a very basic form of power gating.

Stacking power gating technique is applied for each stage of the charge pump design and each stage having the capacitive load of 2pF. The charge transfer switches in the circuit can be completely turned on and turned off, so its pumping efficiency is higher than that of the traditional design.

Our proposed circuit is suitable for applications in low-voltage CMOS processes because of its high pumping efficiency and giving low power consumption. To achieve long-term leakage stacking power reduction is an externally switched power supply is a very basic form of power gating.

The variation of the output amplitude voltage could be obtained from this charge pump of the clock signal to be applied to the input source. The further variation process handled for the low area chip fabrication and for the low power consumption of this proposed charge pump circuit.

Figure 3: Body Biasing With Stacking Power Gating Technique

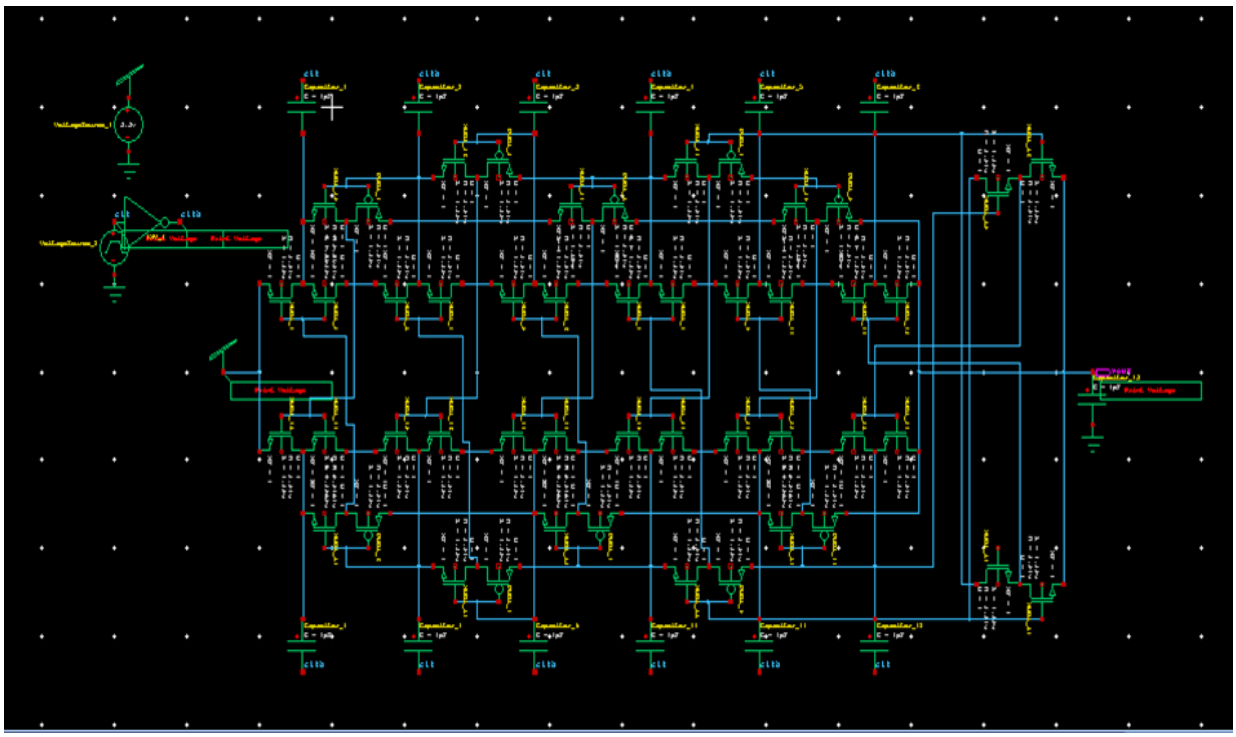


Figure 4: Waveform Specifications of Proposed System

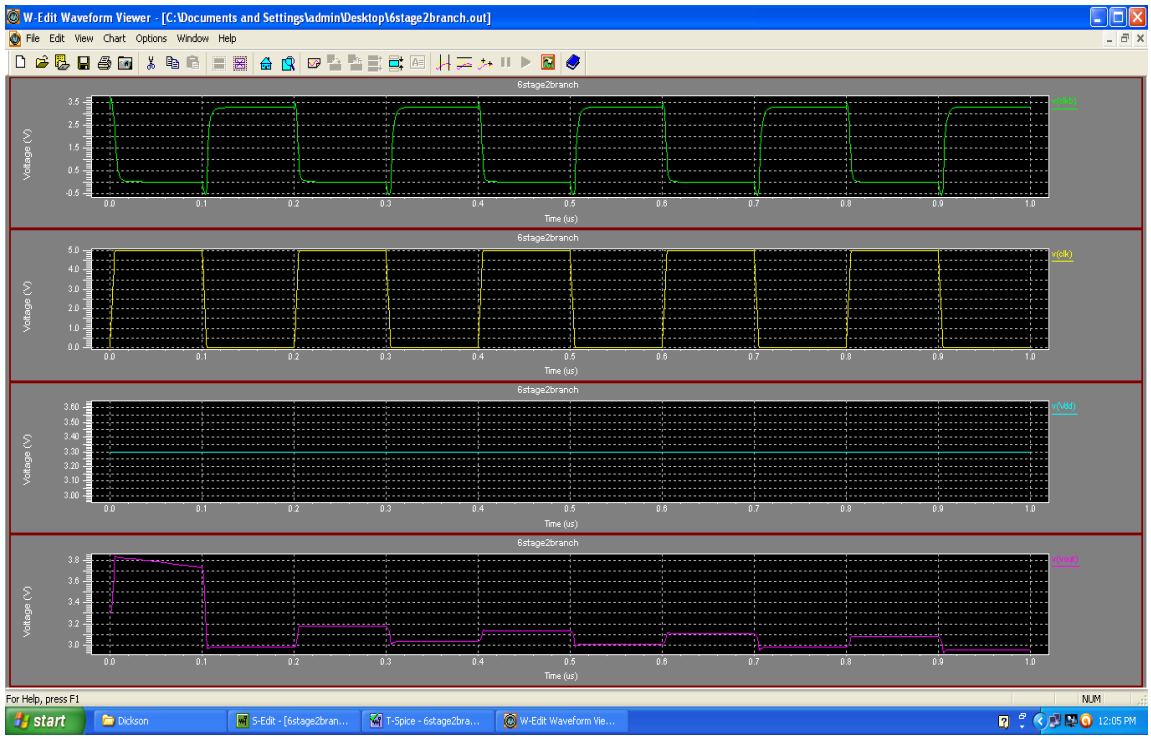


Table 1: Comparsion of Different Charge Pumps

Different Charge Pumps	Number of stages	Input voltage level	Power consumption
Dickson charge pump	6	5V	$3.394e^{-003}$watts
Wu and Chang's charge pump	6	5V	$2.812e^{-003}$watts
Linear charge pump	6	5V	$3.036e^{-003}$watts
Six stage two branch charge pump without stacking power gating	6	320mvto5V	$2.986e^{-003}$wattsto$2.419e^{-002}$watts
Six stage two branch charge pump with stacking power gating	6	320mvto 5V	$1.557e^{-004}$wattsto$1.220e^{-004}$watts

CONCLUSION

Charge pump based on body biasing and the backward control scheme has been proposed.The Stacking power gating technique has been analyzed and the conditions for the important design objectives, i.e. (i) Minimum leakage power; (ii) Minimum low voltage output have been derived. The tradeoff between the leakage power and low voltage has been explored for high-performance stacking power gating logic circuits. A recent trend is towards the CMOS startup charge pump, the power and the amplification could be efficient when compared to the other existing charge pump. The low output ripple and high system stability of the dual-phase charge pump circuit are demonstrated by the test

chip and get better performance. Therefore, the transient response and driving capability can be improved. Besides, only one closed-loop regulation is utilized to generate the charge pump circuit so as to improve the power conversion efficiency. The degradation of the amplification could be highly reduced and it could be generated as per the test identification stages proposed in the charge pump design circuit. Thiscircuit could be further used for the implementation of the like PLL based analog devices. In further it will use another advanced VLSI process. The power consumption of the circuit is (90%) reduced.

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