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Research Paper

A NEW APPROACH TO HIGH EFFICIENCY LOGIC TRANSISTOR BASED SLEEPY SRAM USING 130 NM TECHNOLOGY

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The integrated circuit design has important role of various parameters are considering for design the circuit. The important parameters are power and delay. The different tools are used to perform the operation. However, here the combinational circuit designed by using different logic. As a substitution by using low power design techniques the power consumption is being reduced. Here the low power logic used is sleepy approach. In the sleep approach, an additional “sleep” PMOS transistor is placed between VDD and the pull-up network of a circuit and an additional “sleep” NMOS transistor is placed between the pull-down network and GND. The CMOS leakage current to the process level can be decreased by using sleepy keeper technique. The advantages in this technique are ultra-low leakage with dual V_{th}, state-saving, less area penalty and faster than other techniques like sleepy stack approach, sleep, Zig Zag.

Keywords: RAM, SRAM, DRAM, FET, CMOS

INTRODUCTION

A random-access device allows stored data to be accessed directly in any random order. In contrast, other data storage media such as hard disks, CDs, DVDs and magnetic tape, as well as early primary memory types such as drum memory, read and write data only in a predetermined order, consecutively, because of mechanical design limitations.

An additional driver has been the fact that the software associated with the processors and computers has become more sophisticated and much larger, and this too has greatly increased

the requirement for semiconductor memory. In view of the pressure on memory, new and improved semiconductor memory technologies are being researched and development can be very rapid. Nevertheless, the more mature semiconductor memory technologies are still in widespread use and will remain so for many years to come.

The main idea is to measure the specific cell's currents with variant supply levels via the bit lines. The measured currents are used to estimate the read stability and the write ability through a nonlinear regression. With this alternative stability

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and the cell currents, the conversion rules from currents to the stability can be found from the measurement data. As the conventional techniques cannot be measured without change of the cell structure, alternative metrics are reviewed and their correlations with the conventional stability are discussed (Dong *et al.*, 2008).

A migration technique dynamically moves write-intensive and read-intensive data between STT-RAM and SRAM to explore the advantages of hybrid Cache, the proposed loop retiming technique, the interleaved memory accesses can be significantly reduced so that migration overhead is mitigated, and energy efficiency of hybrid cache is significantly improved (Chen *et al.*, 2010).

Cache memories are used to increase the efficiency of the system by reducing the number of slow and energy-hungry memory accesses. Such applications require high performance occasionally and very little energy consumption during most of the time to extend battery lifetime (Guo *et al.*, 2010).

The doping channel of SRAM transistors are reduced by well proximity and implant shadowing. Stress and doping proximity effects have opposite contributions to device performance. The majority of these simulations were primarily based on either mixed-mode simulation where Technology Computer Aided Design (TCAD) methods are applied to discrete devices, which are connected via a netlist, or TCAD device simulation of full SRAM cells with analytical doping profiles (Driskill, 2011).

The spin-down time, write requests can be temporarily stored in the flash cache, whereas read requests should be carefully handled to avoid

frequent disk spin-ups. This paper presents BEST that make the best use of the hybrid storage to provide low energy consumption, even under many background applications. To make the spin-down time longer, various spin-down techniques have been developed for a few decades in different ways. One of the main purposes of using the flash cache is to reduce the power consumption of a hard disk by eliminating disk activities (Xu, 2011).

Nodes in an ad hoc network have limited power resources as well as limited the processing power. When a routing, a sharp degradation in the network service may result if the routing algorithm does not account for the limited resources, eventually decreasing the lifetime network (Flautner, 2002). To maximize network lifetime, the paths for message flows are chosen in such a way that the total energy consumed along the path is minimized while avoiding the energy in the depleted nodes. To finding the path network which consume minimum energy and finding paths which do not use energy depleted nodes lead to conflicting objectives (Kaxiras, 2001). In contrast to conventional power aware algorithms, the MRPC identifies the capacity of a node just by its residual battery energy, but also been the expected energy spent in reliably packet over forwarding the specific link. The formulation method captures the scenarios of transmission costs also has depend on physical distances between nodes and the link error rates (Jog, 2012).

A realistic power consumption model of the wireless communication subsystems can be typically used in many sensor network node devices is presented. The simple power consumption models for major components are individually identified; the effective transmission

range of the sensor node is modelled by the output power of the transmitting a power amplifier, to sensitivity of the receiving low noise amplifier, and RF environment (Muralimanohar, 2009).

Traditionally, the PSR method is estimated to fraction of successful transmissions over a window of a test packet, to demonstrate that counting based methods do not react to changes in the wireless channel fast enough and that the only way to address this problem is to estimate the PSR based on the receiver's characteristics and on the Signal to Noise Ratio (SNR) at the receiver (Dong *et al.*, 2012).

PRIOR AND RELATED WORK

STT-RAM is used only for the instruction cache and data cache hierarchies are left unmodified. When the processor executes a loop, the instruction cache serves a small number of instructions within the loop body repeatedly until its termination. Therefore, by adding a tiny buffer called a loop cache, instructions for the loop body could be served from the buffer instead of the L1 instruction cache when it can contain the entire loop body.

Loop Cache

A loop cache is a tiny buffer that is used for storing instructions of a small loop body. Trigger branch detection is performed by a simple additional hardware unit; neither the processor nor the target applications need to be modified at all. In addition, a loop cache itself typically does not have a tag array and valid bits because it is used only for loops whose body does not exceed its capacity. This is because, for loops with internal control flows, the counter based controller is not sufficient to determine whether a specific line of a loop cache is valid or not. When the loop cache is accessed, the controller checks whether the

requested address is located inside the loop by comparing it with the boundary address registers.

EXISTING METHOD

Dynamic power has been a predominant source of power dissipation recently. However, static power dissipation is becoming a significant fraction of the total power. Leakage power has become a top concern to the field of VLSI. The leakage problem is worse than generally thought because the simple, traditional leakage power estimation of multiplying the average transistor leakage. Leakage power is primarily the result of unwanted sub threshold current through the transistor channel when the transistor is turned off.

SRAM

SRAM or Static Random Access Memory is a form of semiconductor memory widely used in electronics, microprocessor and general computing applications. This form of semiconductor memory gains its name from the fact that data is held in there in a static fashion, and does not need to be dynamically updated. While the data in the SRAM memory does not need to be refreshed dynamically. SRAM is a type of volatile semiconductor memory to store binary logic '1' and '0' bits. SRAM uses bi stable latching circuitry made of Transistors MOSFETS to store each bit. When the cell is chosen, the value to be written is stored in the cross-coupled flip-flops. A basic SRAM cell consists of two cross coupled inverters forming a simple latch as storage elements and two switches connecting these two inverters to complementary bit lines to communicate with the outside of the cell.

A sense amplifier is an amplifier that senses the output on the bit lines and amplifies it. The sense amplifier that is used in the design is the

'Differential Voltage Sense Amplifier'. It takes small signal differential inputs (i.e., the bit line voltages), and amplifies them to a large-signal single-ended output. The differential approach presents numerous advantages over its single-ended counterpart. One of the advantages is the common mode rejection. It means that such an amplifier rejects noise that is equally injected in both the inputs.

It operates like pass transistors to control the access to SRAM cell by bit lines. The word line controls the functions of SRAM cell. If the WL is high the SRAM cell can be accessed. Otherwise SRAM cell is being isolated. In standby mode the word line WL is low, the access transistors will be off. The data stored in two crossed coupled inverter remain same. There won't be any change in its value as long as supply exists.

Figure 1: Existing Circuit

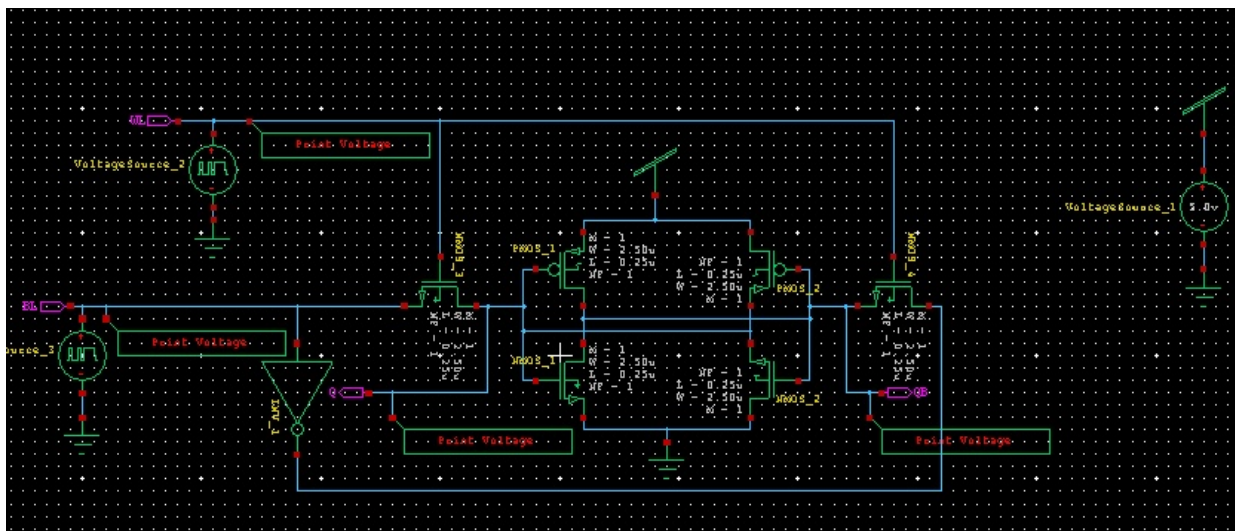
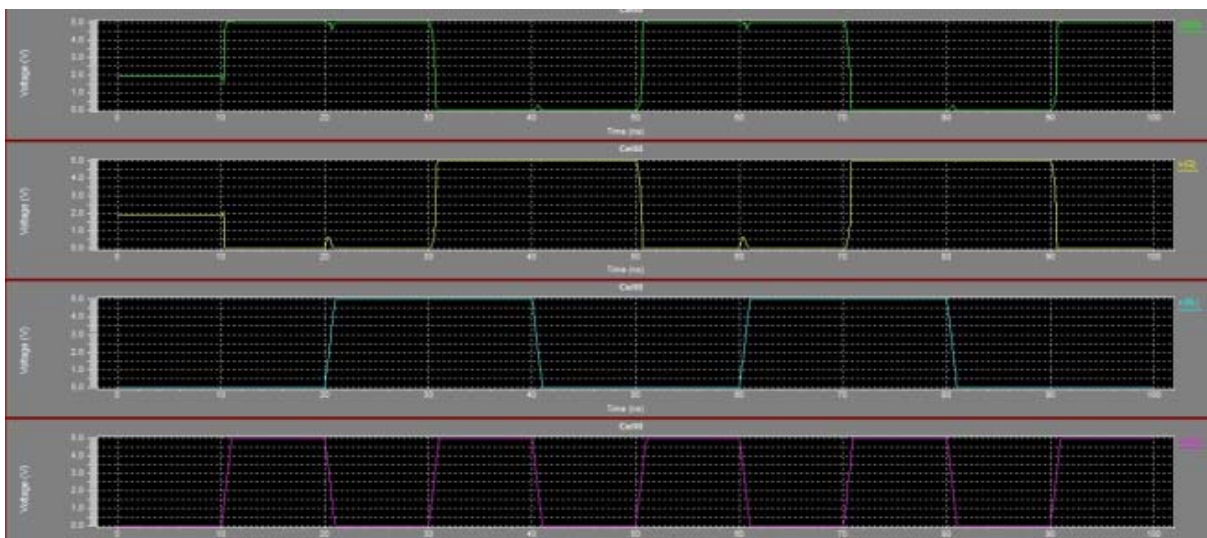


Figure 2: Simulation Output



PROPOSED METHOD

The 10T SRAM cell is the improved form of novel 9T SRAM cell. Here an additional pmos transistor is introduced in between power supply and SRAM cell. This gate connection of this pmos transistor is always grounded. This helps to reduce the power consumption of SRAM cell. For hold condition WL should be high. This produces a low level at the gate of access transistors. This makes access transistors to be isolated from bit lines. For write operation WL should be low.

The dynamic power supply applied should be greater than VDD. Also SEL should be low. Read operation is done by making WL to low and SEL to high. By applying WL=0 the access transistors are turned on. This makes the state stored in SRAM cell to flow towards the bits lines. Before doing this the bits were precharged. This helps to produce variations in voltages in bits lines. These bit lines are being sensed by sense amplifier. The sense amplifier determines which value is stored in it.

Figure 3: Existing Power Value

```

9.922500e-008  5.0000e+000  0.0000e+000  2.1774e-007  5.0000e+000
9.942500e-008  5.0000e+000  0.0000e+000 -1.4959e-007  5.0000e+000
9.962500e-008  5.0000e+000  0.0000e+000  1.7864e-007  5.0000e+000
9.982500e-008  5.0000e+000  0.0000e+000 -1.1483e-007  5.0000e+000
1.000000e-007  5.0000e+000  0.0000e+000  1.4548e-007  5.0000e+000
    
```

* BEGIN NON-GRAPHICAL DATA

Power Results

VVoltageSource_1 from time 0 to 1e-007

Average power consumed -> 1.377521e-003 watts

Max power 1.605469e-002 at time 5.05459e-008

Min power 8.670685e-011 at time 1.6425e-008

* END NON-GRAPHICAL DATA

*

* Parsing 0.01 seconds

* Setup 0.01 seconds

* DC operating point 0.00 seconds

* Transient Analysis 0.11 seconds

* Overhead 1.38 seconds

* -----

* Total 1.50 seconds

* Simulation completed

* End of T-Spice output file

EXPERIMENTAL RESULTS

Existing Model

When their data has been requested, the word line is being made high first. Before that bit lines should be precharged to VDD. As $WL=1$ the cell is being connected to bit lines. According to charge stored in two cross coupled inverters the bit lines will charge or discharge. Then these bit lines are made to reach sense amplifier. The sense amplifier determines the bit stored is 1 or 0.

The term static differentiates it from dynamic RAM (DRAM) which must be periodically refreshed. SRAM exhibits data permanence, but it is still volatile in the conventional sense that data is eventually lost when the memory is not powered. For increasing the battery standby time I am designing a new type of SRAM cell which consumes less power than the existing SRAMs.

Figure 4: Proposed Circuit

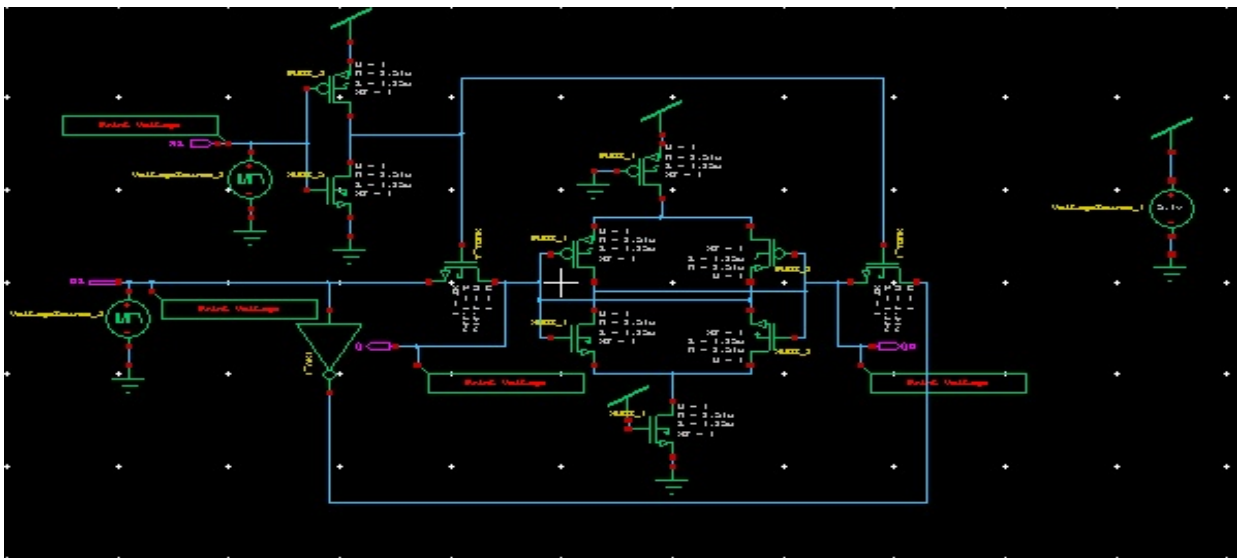


Figure 5: Simulation Output

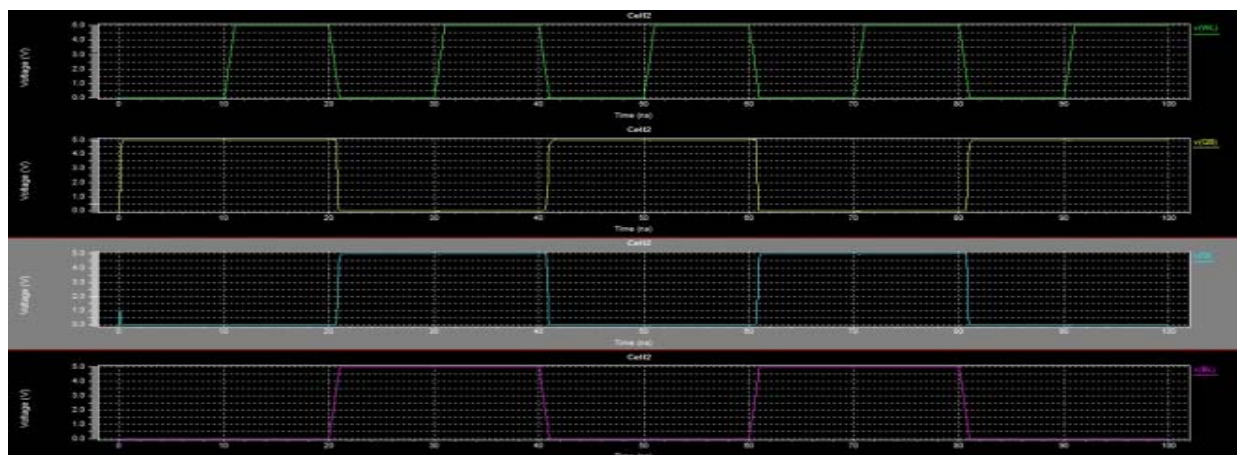


Figure 6: Power Value of Proposed Method

```

9.942500e-008  0.0000e+000  1.3372e-007  5.0000e+000  5.0000e+000
9.962500e-008  0.0000e+000  1.6587e-007  5.0000e+000  5.0000e+000
9.982500e-008  0.0000e+000  1.3687e-007  5.0000e+000  5.0000e+000
1.000000e-007  0.0000e+000  1.6293e-007  5.0000e+000  5.0000e+000

* BEGIN NON-GRAPHICAL DATA

Power Results
/VoltageSource_1 from time 0 to 1e-007
Average power consumed -> 3.806242e-004 watts
Max power 1.994707e-002 at time 7.57183e-011
Min power 0.000000e+000 at time 0

* END NON-GRAPHICAL DATA
*
* Parsing                0.01 seconds
* Setup                  0.01 seconds
* DC operating point     0.06 seconds
* Transient Analysis     0.07 seconds
* Overhead               1.61 seconds
* -----
* Total                  1.76 seconds

* Simulation completed

* End of T-Spice output file

```

CONCLUSION

Thus novel SRAM cells are designed with minimum power consumption and maximum stability in output. The low power design – sleep approach is successfully implemented and the desired result is obtained. This provides us with the minimum power consumption. The newly designed low power memory cells are novel 9T SRAM cell, novel 9T SRAM cell using sleep approach, 8T SRAM cell using sleep approach and novel 10T SRAM cell. A power reduction of 43% is obtained for novel 10T SRAM cell for write operation. 40% of power consumption is reduced for write operation and 11 % for read operation

for 8T SRAM cell using sleep approach is obtained.

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