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Research Paper

DESIGN OF LOW POWER AND HIGH SPEED DOUBLE TAIL COMPARATOR USING CLOCK GATING METHOD

R Manopriya[1]* and M Karthik[2]

Corresponding Author: R Manopriya ✉ manomadhi@gmail.com

Comparators are the basic elements for designing the modern analog and mixed signal systems. The speed and area is main factors for high speed applications. Various types of dynamic double tail comparators are compared in terms of Delay, Area, Power, Glitches, Speed and average time. The accuracy of comparators it mainly defined by its power consumption and speed. The comparators are mainly achieving the overall higher performance of ADC. The high speed comparators suffer from low voltage supply. Threshold voltage of the device is not scaled at the same time, as the supply voltage of the device. In modern CMOS technology the double tail comparator is designed by a using the dynamic method, it mainly reduces the power and voltage. The analytical expression method it can obtain an intuition about the contributors, comparator delay and explore the trade-off dynamic comparator design.

Keywords: Double Tail comparator, ADC, Dynamic comparator, Glitches

INTRODUCTION

Comparators have essential influence on the overall performance in high speed Analog to Digital Convertors (ADCs). In wide-ranging a comparator is a device, which compares two currents or voltages and produces the digital output based on the comparison. Since comparators are usually not used with the feedback there is not compensation so neither the area reduction or speed reduction value is invited. Comparators are known as 1-bit analog to digital converter and for that reason they are mostly used in large quantity in A/D converter Dynamic comparators are widely used in the design of high speed ADCs. Due to speed, low power consumption, high input impedance and full swing output, the dynamic latched comparators are very attractive for many kinds of applications such as high speed ADCs, memory sense amplifiers. Increasing packing densities coupled with faster clock frequencies has forced the issue of heat removal and power dissipation to the forefront of virtually every mainstream design application under the SUR.

[1] P.G. Scholar, CMS College of of Engineering, Namakkal, Tamil Nadu, India.
[2] Assistant Professor, CMS College of of Engineering, Namakkal, Tamil Nadu, India.

And the problem is predicted to continue to be a major challenge in the coming decade as we approach Giga Scale Integration (GSI) (Ay, 2011). Analogue to digital conveners are one of the main building blocks of most portable electronic equipments, such as cell phones, electronics products. They increasing demand of longer battery life time of portable equipments has forced circuit designers to use lower supply voltages. However the supply voltage is lowered the performance of analogue circuits is degraded and the design of low voltage analogue Circuits becomes more challenging. The AX analogue-to-digital conveners are very suitable for low voltage applications (Babayan *et al.,* 2012).

It consists of a front end sampler a regenerative stage, and a clocked amplifier is to provide a small aperture time and high toggle rate. Then the clocked amplifier employs a bandwidth modulation technique that switches the feedback gain to reduce the reset time while keeping the effective gain high (Blalock, 2000). There are several fields of application for comparators. In flash ADCs many clocked comparators decide in parallel for fast analogue-to-digital conversion. So, the demands on such comparators are mostly low power consumption and a high sampling rate, while a small chip area is occupied. To have always the same capacitive loads at both outputs of the comparator, the buffer has two parallel first stages and with the digital pin SW the second stage in the buffer can be switched. The buffer was designed with an attenuation of a factor of two to enhance the bandwidth and to achieve a good linearity for the overall buffer (Goll, 2011). It is now a challenge to develop new circuit structures that either avoid a stack of too many transistors between the supply rails, so that the technology-given better ac performance does not degrade, or keep the advantages of standard circuits, a new latch for low-supply-voltage operation, where the advantages of a high-impedance input, a rail-to-rail output swing, no static power consumption (Goll, 2009).

This technique is very suitable for very-low power clocked and continuous time circuits such as level shifters, Op-amp and comparators. Design of a 10-bit Supply Boosted (SB) SAR ADC is presented as an example of the technique. Voltage design techniques such as clock boosting were also used. A unique supply and clock booster was designed as integral part of new supply boosted comparator. Input common mode range of SB comparator was extended by using supply boosted level shifter circuits (Goll, 2009). Among the key performance metrics of a dynamic latch used in a voltage comparator is its input referred offset voltage. Relevant effects that contribute to the offset can be divided into static and dynamic components. The most commonly discussed source of static offset stems from threshold voltage mismatch in the constituent transistors. Two simple equations for predicting the offset were derived and compared against simulation data (Goll, 2007).

The degeneration resistors are the latching pair and it's to reduce transistor charging time for regeneration. Charging time, they allowing more time for regeneration. The introduction method consists of the emitter degeneration resistors in the latching pair. The degeneration resistors reduce the transistor charging time, providing more time for the critical process of regeneration. As the latching pair is isolated from the input nodes degenerates still improves the sensitivity when a preamplifier is used (He, 2009). To overcome the challenges associated with to reduce the supply voltage, a double tail latched comparator with a variable capacitance, calibration technique they using a metal oxide metal capacitors is implemented. An all-digital time domain delay interpolation technique further enhances the resolution with very little additional power consumption (Mayamandi, 2003).

CONVENTIONAL DYNAMIC COMPARATOR

The double tail comparator achieves the better performance and the double tail comparator and the architecture it mainly used in the better performance used in the low voltage applications. The comparator designed based on double tail architecture. The main idea of this method is to increase $\Delta Vfn/fp$ is to increase the latch regeneration speed. The main operation of the comparator is during reset phase CLK = 0, Mtail1 and Mtail2 is off, to avoiding these static power, M3 and M4 switches pulls both fn and fp nodes to VDD. Hence, the transistor Mc1 and Mc2 are cut off, intermediate stage transistors MR1 and MR2 is reset both latches outputs to ground. During decision making phase CLK = VDD. Mtail1 and Mtail2 are on transistors M3 and M4 turn off. Furthermore, at the beginning of the phase, the control transistors are still off. Thus, fn and fp start to drop with different rates according to the input voltages. The second term, *t*latch, is the latching delay of two cross coupled inverters. It is assumed that a voltage swing of *V*out = *V*DD/ 2 has to be obtained from an initial output voltage difference V0 at the falling output. This is a self biasing differential amplifier. An inverter was added at the output of the amplifier as an additional gain stage, to isolate any load capacitance from the self biasing differential amplifier.

The size of M1 and M2 are set by considering the differential amplifier's transconductance and the input capacitance. The transconductance sets the gain of the stages, while the input capacitance of the comparator is determined by the size M1 and M2. Similar to the conventional dynamic comparator, the delay of this comparator comprises two main parts, t0 and tlatch. The delay t0 represents the capacitive charging of the load capacitance CL out (at the latch stage output nodes, Outn and Outp) until the first n-channel transistor (M9/M10) turns on, after which the latch regeneration starts; thus t0 is obtained where IB1 is the drain current of the M9 and approximately equal to the half of the tail current. Thus, it can be concluded that two main parameters which influence the initial output differential voltage and thereby the latch regeneration time are the transconductance of the intermediate stage transistors (*g*mR1,2) and the voltage difference at the first stage outputs (fn and fp) at time *t*0.

PROPOSED DOUBLE TAIL COMPARATOR

To achieve the better performance of double tail architecture in low voltage applications, the proposed method comparator is designed based on the double-tail structure.

Operation of Proposed Comparator

1. Reset Phase: Clk = 0, Mtail1and Mtail2 OFF. For this process static power is avoided. np and nf nodes to VDD. Latches to be Ground.
2. Decision making phase: Clk = VDD, Mtail1 and Mtail2 are ON, M3 and M4 OFF.

During reset phase clk=0, Mtail1 (M3) and Mtail2 (M20) are OFF, M10 and M13 will pull both fn and fp nodes to VDD. Hence MC (M11) and MC (M12) are cut off, M6 M9 are discharge to output nodes to VSS. During an decision making phase clk =VDD, Mtail1(M3) and Mtail2(M20) are ON, transistor M10 and M13 will OFF and fn and fp nodes are start drop with different rates according to input voltage. VINP>VINN means fn is faster than fp, M15 transistor provide more current than M14. MC (M11) is turn on, fp node pulling back to VDD MC (M12) remains OFF, fn node discharged. Offset will low and delay reduced. Parallel connected dynamic latch is used as load of first stage to increase voltage difference due to cascade connection delay will more compare to parallel connection. The latch of this first stage start regenerating depending on the input differential voltage (Vin1, Vin2), producing a large difference voltage. This difference voltage is sense at the second stage input and the second stage latch regenerate output voltage Out1 and Out2. As fast sensing it is exploiting less time to produce output when compare to previous work. It consumes less power compared to conventional one. As the way delay has reduced.

EXPERIMENTAL RESULTS

Existing Model

In order to compare the proposed comparator with the conventional and double tail dynamic comparator all circuits have been simulated in a 130 nm CMOS technology the post layout simulation have been simulated in Tanner EDA which is used to calculate the area of the conventional dynamic comparator as shown in Figure 1, Double tail dynamic comparator as in Figure 3 proposed double tail dynamic comparator.

Circuit Diagram

Due to the fact that parasitic capacitances of input transistors do not directly affect the switching speed of the output nodes, it is possible to design large input transistor to minimize the offset. The disadvantage, on the other hand, is the fact that due to several stacked transistors, a sufficiently high supply voltage is needed for a proper delay time. The reason is that, at the beginning of the decision, only transistors *M*3 and *M*4 of the latch contribute to the positive feedback until the voltage level of one output node has dropped below a level small enough to turn on transistors *M*5 or *M*6 to start complete regeneration.

Figure 1: Existing Dynamic Comparator

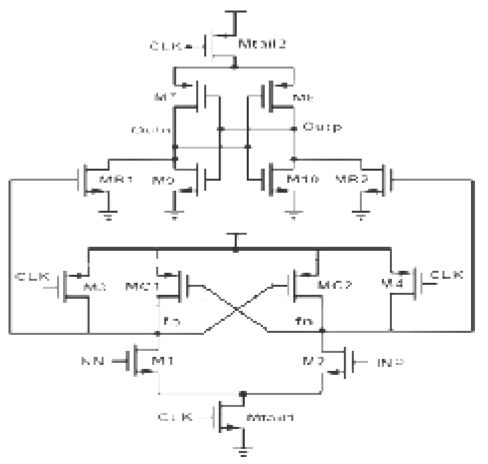
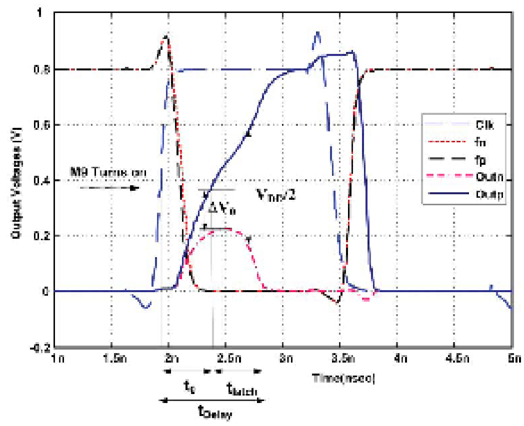


Figure 2: Energy Diagram of Existing System

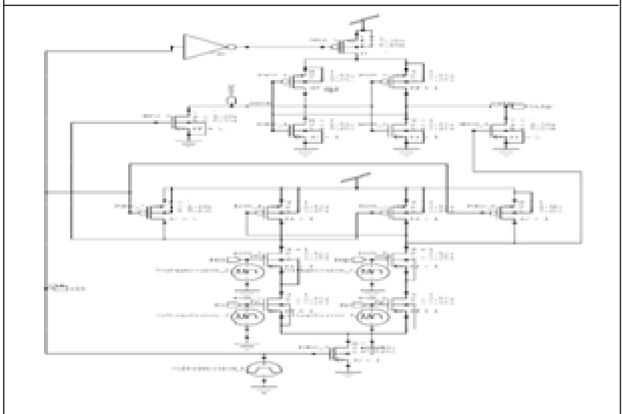


Graph Output

Proposed Method

As long as fn continues falling, the corresponding PMOS control transistor (*M*c1 in this case) starts to turn on, pulling fp node back to the *V*DD; so another control transistor (*M*c2) remains off, allowing fn to be discharged completely. In other words, unlike conventional double-tail dynamic comparator, in which *V*fn/fp is just a function of input transistor transconductance and input voltage difference in the proposed structure as soon as the comparator detects that for instance node fn discharges faster, a PMOS transistor (*M*c1) turns on, pulling the other node fp back to the *V*DD.

Figure 3: Proposed Circuit



Circuit

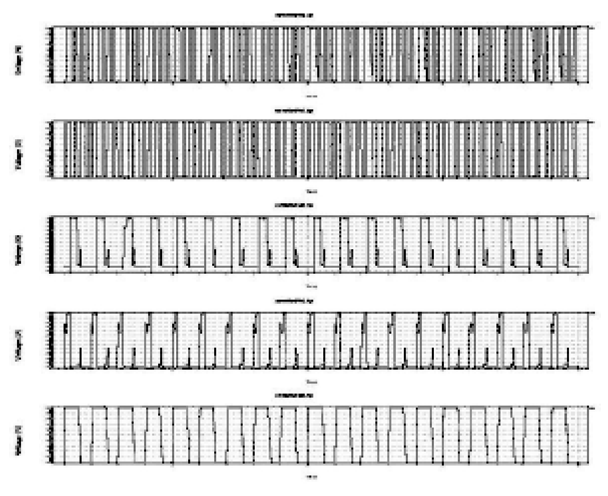
Therefore by the time passing, the difference between fn and fp (*V*fn/fp) increases in an exponential manner, leading to the reduction of latch regeneration time.

It is evident that the double-tail topology can operate faster and can be used in lower supply voltages, while consuming nearly the same power as the conventional dynamic comparator. The case is even much better for the proposed comparator when compared to the conventional double-tail topology.

Parsing	0.10 s
Setup	0.01 s
DC operating point	0.00 s
Transient Analysis	1.14 s
Overhead	2.01 s
Total	3.26 s

Simulation Graph

Figure 4: Proposed Output



CONCLUSION

This work presents that comprehensive delay analysis for clocked dynamic comparators. Two common structures of conventional dynamic comparator and conventional double- tail dynamic comparators have been analyzed. A new dynamic comparator with low-voltage low-power capability has been proposed in order to improve the performance of the comparator and also reduces the delay. The area estimation is evaluated using post layout simulation with the help of micro wind simulator.

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Hyderabad, INDIA. Ph: +91-09441351700, 09059645577
E-mail: editorijlerst@gmail.com or editor@ijerst.com
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