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Research Paper

IMPLEMENTATION OF POWER EFFICIENT 20-GHZ RSFQ MULTIPLIER

Srinivas Sapa[1]* and P Balanagu[2]

*Corresponding Author: ***Srinivas Sapa*** ✉ srinivasu472@gmail.com

The growing market for fast floating-point coprocessors, digital signal processing chips, and graphics processors has created a demand for high speed, area efficient multipliers. Current architectures range from small, low-performance shift and add multipliers, to large, high-performance array and tree multipliers. Conventional linear array multipliers achieve high performance in a regular structure, but require large amounts of silicon. Tree structures achieve even higher performance than linear arrays but the tree interconnection is more complex and less regular, making them even larger than linear arrays. Ideally, one would want the speed benefits of a tree structure, the regularity of an array multiplier, and the small size of a shift and add multiplier. In electronics, rapid single flux quantum (RSFQ) is a digital electronics technology that relies on quantum effects in superconducting devices, namely Josephson junctions, to process digital signals. Josephson junctions are the active elements for RSFQ electronics, just as transistors are the active elements for semiconductor electronics. However, RSFQ is not a quantum computing technology in the traditional sense. Even so, RSFQ is very different from the traditional CMOS transistor technology used in every day computers due to its power efficiency and high speed it is being used.

Keywords: RSFQ, Carry Save Adder, Verilog

INTRODUCTION

It is based on superconductors, so a cryogenic environment is required the digital information is carried by magnetic flux quanta that are produced by Josephson junctions instead of transistors in semiconductor electronics the magnetic flux quanta are carried by picoseconds duration voltage pulses that travel on superconducting transmission lines, instead of static voltage levels in semiconductor electronics. Consequently the area of the quantized voltage pulses that carry single magnetic flux quanta is constant. Depending on the parameters of the Josephson junctions, the pulses can be as narrow as 1 pico-second with an amplitude of about 2 mV, or broader (typically 5–10 picoseconds) with a lower

[1] M.Tech. Student, Department of ECE, Chirala Engineering College, Chirala 523155, Prakasam Dt., AP.
[2] Associate Professor, Department of ECE, Chirala Engineering College, Chirala 523155, Prakasam Dt., AP.

amplitude since pulses usually propagate on superconducting lines, their dispersion is limited and usually negligible if no spectral component of the pulse is above the frequency of the energy gap of the superconductor in 2010, the typical values of the maximum pulse amplitude, usually called the IcRn product, is of the order of 0.5 to 1 mV. Rn is the normal resistance of the Josephson junction that generates the voltage pulses, while Ic is its critical current. In the case of pulses of 5 picoseconds, it is typically possible to clock the circuits at frequencies of the order of 100 GHz (one pulse every 10 picoseconds).See also: Quantum flux parametron, a related digital logic technology.

BASIC MULTIPLIERS

In any multiplication algorithm, the operation is decomposed in a partial product summation. Each partial product represents a multiple of the multiplicand to be added to the final result. Nowadays almost all high-speed multipliers apply a radix-4 recoding multiplication algorithm. Radix-8 recoding allows a time gain in the partial products summation but it is not applied because we have to generate one of the multiples of the multiplicand (an odd multiple) using a high-speed adder (the previous adder).

High speed multiplication is a primary requirement of high performance digital systems. In recent trends the column compression multipliers are popular for high speed computations due to their higher speeds. The first column compression multiplier was introduced by Wallace in 1964. He reduced the partial product of *N* rows by grouping into sets of three row set and two row set using (3,2) counters and (2,2) counters respectively.

In 1965, Dadda altered the approach of Wallace by starting with the exact placement of the (3,2) counters and (2,2) counters in the maximum critical path delay of the multiplier. Since 2000's, a closer reconsideration of Wallace and Dadda multipliers has been done and proved that the Dadda multiplier is slightly faster than the Wallace multiplier and the hardware required for Dadda multiplier is lesser than the Wallace multiplier. Since the Dadda multiplier has a faster performance, we implement the proposed techniques in the same and the improved performance is compared with the regular Dadda multiplier.

RFSQ

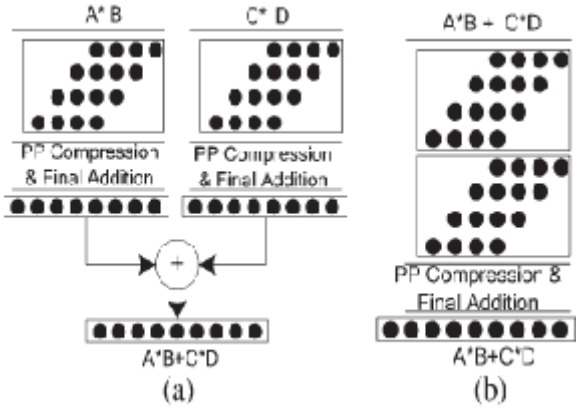
The benefit of the Wallace tree is that there are only O (log n) reduction layers, and each layer has O (1) propagation delay. As making the partial products is O (1) and the final addition is O (log n), the multiplication is only O (log n), not much slower than addition (however, much more expensive in the gate count). Naively adding partial products with regular adders would require O ($\log^2$ n) time. From a complexity theoretic perspective, the Wallace tree algorithm puts multiplication in the class NC. These computations only consider gate delays and don't deal with wire delays, which can also be very substantial. The Wallace tree can be also represented by a tree of 3/2 or 4/2 adders.

PP TRUNCATION AND COMPRESSION:

Design of FIR filter is adopted in direct with this easy. Is - [i in n] products ai × X where all collectively MCMA module 1 (a). Alternatively, instead of accumulating the multiplication of the individual for each product, and to PPB matrix

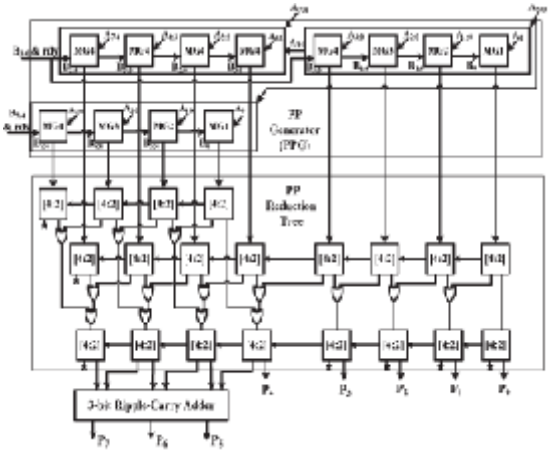
with a single carry-save addition in order to reduce the height of the matrix of the two following the carry propagation adder final. If you collect all of the PP is more efficient. Figure shows the multiplication of the combination and the difference of the multiplication of the individual 4.1 × B + C × D.

Figure 1: Multiplication/accumulation Using (a) individual PP compression and (b) combined PP compression



To avoid sign extension bits to complement the sign bit of each PP column, as shown in the figure, with the S = 1~s of the property is the sign bit of the PP column, s is a constant I biasing few. All bias constants are collected in the last row of the matrix PPB. It is shown by white circles on the rod of the complement of the PPB. Generation of PPBs considering sign extension and negation. That the implementation of the FIR filter rounded faithfully is introduced between the arithmetic operations, the total error is greater than anyone ULP is not required. We will change the design of truncation multiplier of recent lead in a small area cost you can delete the PPB more and more, in as compares the two approaches. In, removal of PPB of unnecessary is made up from three processes. Delete, truncation, and rounding. Two rows of PPB to be removed by rounding or truncation of then are set to delete not them. After you add a constant offset of the deletion, truncation, are given as follows:

Figure 2: 20 GHZ Multiplier Diagram



Truncated multiplier designs using (a) the approach in and (b) the improved version. The figure 2 the circle of gray, and crossed the green circle, respectively, a red circle shows an example of the approach in Over represents Delete bit, the truncation bit, rounding a bit. As can be seen, with this easy proposes a improved version of the truncation rounded multiplier design faithfully. It is shown in fig (For subsequent rounding) is performed irremovable, a single row of PPB dedicated, are made up of rounded and delete only the removal of the PPB. Error range Delete as follows, rounding in the improved version is as follows. For the range of deletion errors is twice than to be able to delete the PPB more with an improve version, which leads to a smaller area in PPB compression of trailing overall FIR filter architecture using multiple constant multipliers/ accumulators with faithfully rounded truncation (MCMAT).

Shows an exemplary architecture of the MCMA (MCMAT) truncated to remove the PPB

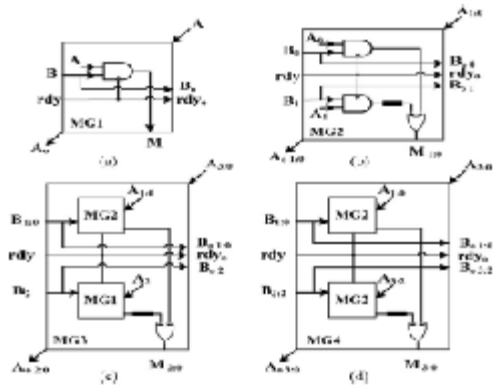
unnecessary. White circle of the L-shaped block represents the PPB undeletable. Deletion of the PPB is represented by a gray circle. After the PP compressed, and are shown by circles rounding of bits obtained intersects. Such as changing the sign bit, constant bias and offset all of the last row of the matrix represents PPB is required.

In the 8 × 8-bit multiplier. The multiplier consists of three major blocks: a partial product generator, a parallel carry-save partial reduction (compression) tree, and a ripple-carry adder for final summation of carry-sum operands for the three most significant bits. A.

PARTIAL PRODUCT GENERATOR WITH 80-GHZ OUTPUT STREAMS:

The multiplier partial product generator (PPG) consists of36 partial product (PP) bit generators built with clocked AND gates operating on their multiplicand and multiplier bits. These circuits are organized into three PPG groups, one (top left) with 16 and two other with 10 PP generators each. PPs in each PPG group are calculated in parallel, significantly reducing the partial product generation time. The PPG groups are implemented with four different types of modules

Figure 3: PP Generation Modules



MG1–MG4 with their indexes corresponding to the number of PPs generated by the modules When generated, PPs within each MG are merged together with confluence buffers (implementing asynchronous OR operations) and sent <“12.5 ps apart over a single passive transmission line (PTL) to their first-level [4:2] compressor.

The minimum time gap of 11–12 ps between PP signal pulses is necessary to meet timing constraints and provide some DC bias margins of the confluence buffers and [4:2] compressors. The required time separation between PPs is achieved with a use of carefully designed operand and control distribution networks utilizing JJ-based delay lines, parallel and serial signal splitting. Working in parallel, the 12 MG blocks asynchronously generate and send PPs (36 total) to the [4:2] compressors at the “hardwired” rate of 80 GHz.To reduce (compress) partial products in each column, we use a two-level binary carry-save reduction tree built with [4:2] compressors (see Figure 4). First, up to 8 PPs in each column are reduced to 4 by two [4:2] compressors working in parallel, each producing 2 PPs. The 4 PPs from the two first-level compressors are merged together with asynchronous confluence buffers and sent <“12.5 ps apart over a single PTL to a second-level [4:2] compressor for that column. Then, the second-level [4:2] compressor will reduce those 4 PPs to 2.The benefits of using this approach are as follows: 1) the O(log2n) PP reduction time, where n is the operand length, and 2) a regular layout. The latter is very important for our 80-GHz asynchronous data-driven wave-pipelined implementation of the [4:2] compressors.

Addition is a fundamental operation in many VLSI systems such as application specific DSP architectures and microprocessors. Full adder is fundamental unit in various circuits, especially, in performing arithmetic operations such as compressors, comparators, parity checkers, multipliers etc. It is the nucleus of many other useful operations such as subtraction, multiplication, division, exponentiation, address calculation and can significantly influence the overall achievable performances of the system. At the same time, the sustained massive growth of the mobile appliances market is pushing the demand for power-efficient VLSI circuits. For this reason, low power high speed adders are highly desirable. The role of full adders in arithmetic circuits can be classified into two categories: The chain structured such as ripple carry adders (RCA) and array multipliers. In these applications, the critical path often traverses from the carry input to the carry output of the full adders. It is demanded that the generation of the carry-out signal is fast. Otherwise, the slower carry-out generation will not only extend the worst case delay, but also create more glitches in the later stages, hence, consume more power. The tree structured, which is frequently used in multipliers. A multiplier is typically composed of three stages- Partial products generation stage, partial products addition stage, and the final addition stage. In the first stage, the multiplicand and the multiplier are multiplied bit by bit to generate the partial products. The second stage is the most important, as it is the most complicated and determines the speed of the overall multiplier. The 4-2 compressor has been widely employed in the high speed multipliers for the construction of Wallace tree to lower the delay of the partial product accumulation stage. The addition of the partial products contributes most to the overall delay, area and power consumption, due to which the demand for high speed and low power compressors is continuously increasing. A. 1-bit full adder

A 1-bit full adder is a combinational circuit that performs the arithmetic sum of three bits. It consists of three inputs a, b and cin and two outputs sum and carry. Expressions for sum and carry are;

$$Sum = a \oplus b \oplus cin \quad (1)$$

$$carry = a \oplus b \oplus cin + ab \quad (2)$$

The block diagram of 1-bit full adder, as shown in Figure 1 is used as a basic building block in many VLSI circuits and systems such as comparators, parity checkers, ripple carry adder (RCA), carry skip adder, carry select adder, array multiplier, 4-2 compressor and microprocessors etc Thus, enhancing the performance of the 1-bit full adder block leads to the enhancement of the overall system performance.

RESULTS

Figure 4: 20ghz Multiplier Waveform

Figure 5: RTL Schematics

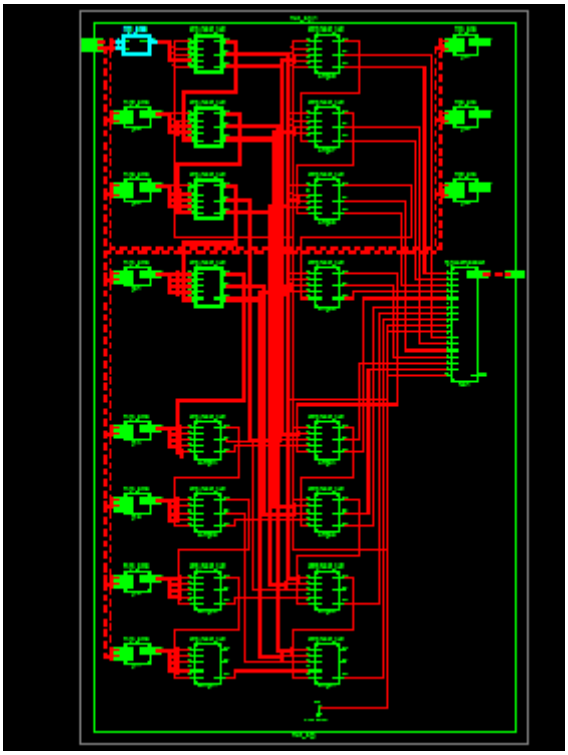
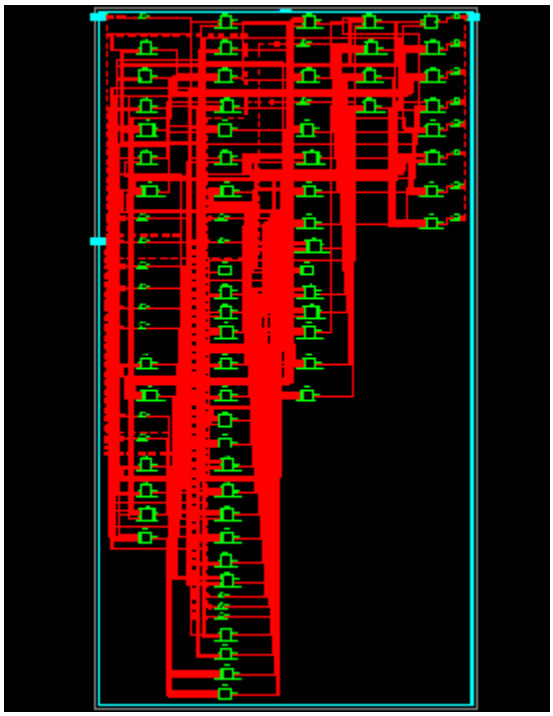


Figure 6: Technology Schematics



CONCLUSION

In electronics, rapid single flux quantum (RSFQ) is a digital electronics technology that relies on quantum effects in superconducting devices, namely Josephson junctions, to process digital signals. Even so, RSFQ is very different from the traditional CMOS transistor technology used in every day computers due to its power efficiency and high speed it is being used. The functionality is verified using ISE simulator and the synthesis is carried out using XILINX ISE 12.3i with VERILOG HDL. The Total memory usage is 135684 kilobytes. The time required to generate the output after applying the input is 18.227ns with the utilized 4 input LUTs of 62 and the consumed power of 0.50548mw.

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