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Research Paper

WIRE REDUNDANCY IN BUS ENCODING TECHNIQUES FOR FORBIDDEN TRANSITIONS FREE CROSS TALK AVOIDANCE CODEC DESIGNS

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A simple technique to eliminate crosstalk delay in DSM Technology is by placing a shielding wire between every adjacent wire. But this technique has a drawback of doubling the wiring area. Several Bus Encoding Techniques have been proposed by several authors to eliminate/reduce crosstalk delay in VLSI inter connects without placing a shielding wires. Some of these methods are based on routing strategies, which employ various routing techniques to minimize crosstalk delay within a data-path or logic block. The main idea is to prevent simultaneous opposite transitions by skewing signal transition timing of adjacent wires. The crosstalk is dependent on the data transition patterns on the bus, patterns can be classified based on the severity of the crosstalk they impose on the bus. The general idea behind techniques that improve on-chip bus speed is to remove undesirable patterns that are associated with certain classes of crosstalk. Different schemes incur different area overheads since they require additional wires, spacing between wires or both. The number of bits used for the representation of encoding information is high. Encoding all the data irrespective of the presence of forbidden patterns leads to some unwanted crosstalk. The bus encoding schemes in the literature, that describes forbidden transitions free crosstalk avoidance CODEC designs, does not address the area overhead caused by extra wires and calculates bus energy dissipation based on this premise. It does not evaluate an encoding method's viability from the perspectives of crosstalk noise and noise-induced delay. We compare the area over head required for various bus encoding schemes that describes forbidden transitions free cross talk avoidance CODEC designs and we propose certain modifications for achieving more reduction in power and crosstalk delay with least energy over head in redundant wires.

Keywords: DSM, VLSI, Forbidden transition free patterns, CODEC

INTRODUCTION

The increasing prominence of portable systems, like notebook computers, portable communication devices demanding high chip density and high throughput along with low power consumption. Now a days reducing the power consumption has

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become an important objective in the design of digital integrated circuits. This can be done through design improvements. The total power consumption is divided among four major parts.

1. Logic circuits
2. Clock generation and distribution
3. Interconnections; and
4. Off-chip driving (I/O circuits).

The two main sources of power dissipation in VLSI circuits are static power and dynamic power. Static power (Jan M Rabaey *et al*., 2003) results from resistive paths between power supply and ground. The static power dissipation of a circuit is expressed by the relation

$$P_{stat} = I_{stat} V_{DD} \quad ...(1)$$

where, I_{stat}

I_{stat} is the current that flows between the supply rails *n* the absence of switching activity

Dynamic power results from switching capacitive loads between different voltage levels.

For a CMOS gate the dynamic power is

$$P_{dynamic} = \alpha C V_{DD} 2\frac{1}{\tau} \quad ...(2)$$

where, α is the activity factor of the output nodes.

C is the total capacitance of the output nodes.

V is the supply voltage.

τ is the delay or time period.

For a complex chip, the total dynamic power is the sum of the dynamic power of all the gates. Resultant equation is same as Equation (2). The only difference is *C*, the total capacitance of all the loads and the activity factor, which is the average activity factor. So, Equation (2) is modified as

$$P_{dynamic} = \alpha C_{eff} V_{DD} 2\frac{1}{\tau} \quad ...(2.1)$$

By summing up these two dissipations, total power dissipation is not obtained. Still there is some difference which is caused by two other factors, i.e., due to the short circuit current and the leakage current. Short circuit current results from both the transistors in a CMOS inverter being ON at the same time when the input switches and there are four main sources of leakage current in CMOS transistor (Farman Fallah and Massoud Pedram, 1995). They are

1. Reverse-biased junction leakage current (I_{REV})
2. Gate induced drain leakage (I_{GIDL})
3. Gate direct-tunnelling leakage (I_G)
4. Sub threshold (weak inversion) leakage (I_{SUB})

Thus, the total power dissipation in CMOS digital circuits can be expressed as the sum of four components (Sung-mo kang and Leblibici)

$$P_{total} = \alpha C_{load} V_{DD}^2 1/\tau + V_{DD}(I_{(short\text{-}circuit)} + I_{leakage} + I_{static}) \quad ...(3)$$

where, $I_{short\text{-}circuit}$

$I_{short\text{-}circuit}$ = average short circuit.

$I_{leakage}$ = reverse leakage and sub threshold current.

I_{static} = DC current component drawn from the power supply

The first term in the Equation (3) is the dominating component in most CMOS logic circuits (which is due to dynamic power) because it is proportional to the switching frequency, which we are increasing rapidly to improve the speed

of the circuit. The effect of the remaining terms on the circuit is very less. So, they can be ignored (Chatterjee *et al.,* 1996; Sotiriadis and Anantha Chandrakasan, 2002).

Device characteristics (e.g., threshold voltage), device geometrics, and interconnect properties are significant factors in lowering the power consumption. Circuit-level measures such as the reduction of voltage swing, clocking strategies can be used to reduce power dissipation at the transistor level. The power consumed by the system can be reduced by minimizing the number of switching events for a given task.

We have several means for reducing the power consumption.

1. Reduction of the power supply voltage.
2. Reduction of voltage swing in all nodes.
3. Reduction of the switching probability (transition factor).
4. Reduction of the load capacitance.

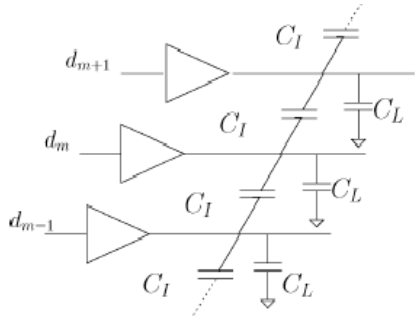
Switching power dissipation is also a linear function of the clock frequency .But reducing it diminishing the overall system performance. Thus, the reduction of clock frequency would be a viable option only in cases where the overall throughput of the system can be maintained by other means. The load capacitance can be reduced by using certain circuit design styles and by proper transistor sizing. The reduction of switching activity requires a detailed analysis of signal transition probabilities, and implementation of various circuit-level and system level measures such as logic optimization, use of gated clock signals, and prevention of glitches.

DEEP SUB MICROMETER DESIGN

Once the design of VLSI technology has moved on to the regime of Deep Sub Micrometer design (DSM) interconnect delay has become a major hurdle. Crosstalk has become the major factor of the total power consumption and the time delay. Bus encoding can be used to reduce crosstalk. Interconnect delay has dominated the logic delays. A simplified on chip bus model with crosstalk is considered which is shown in Figure 1.

In Figure 1 C_L denotes the load capacitance which is seen by the driver which includes the receiver gate capacitance and also the parasitic wire to substrate parasitic capacitance. C_I is the inter wire coupling capacitance between adjacent lines of the bus. Reducing the crosstalk boosts the speed of the bus significantly (Sotiriadis and Anantha Chandrakasan, 2001, 2002 and 2003).

Figure 1: On-Chip Bus with Crosstalk



Delay in a bus of the j^{th} wire is given by Equation (4)

$$T_j = abs\ (k.C_L.\Delta V_J + k.C_I.\Delta V_{j,j-1} + k.CI.\Delta V_{j,j+1}) \quad ...(4)$$

K is the constant determined by the driver strength and wire resistance. ΔV_j is the voltage change on the j^{th} line and $\Delta V_{j,k}$ is the relative voltage between the j^{th} and the k^{th} line.

FORBIDDEN PATTERNS [8,9]

Forbidden patterns are defined as 3 bit patterns “101” and “010". Any data or a code that represents the data is said to be Forbidden Pattern Free (FPF) if there are no forbidden patterns in any three consecutive bits.

Fibonacci numeral system was first used in Forbidden transitions free crosstalk Avoidance CODEC designs by authors Chunjie Duan *et al.* (2004) and (2009) to minimize crosstalk delay in DSM Technology. Fibonacci numeral system is the numeral system that uses the Fibonacci sequence as the base. Any number can be represented as the summation of the Fibonacci numbers.

Several different schemes have been proposed for CODEC construction for FPF-CAC or other memory-less CAC’s. These schemes are all based on bus partitioning. This breaks up a wide bus into smaller groups or lanes (typically 3 to 5 bits) and exhaustively searches for the optimal mapping that yields the most efficient CODEC for the groups. Unfortunately, in order to handle crosstalk across the group boundaries, these schemes all inevitably suffer from additional area overhead.

COMPARISON OF ENERGY OVERHEAD FOR CODEC AT VARIOUS BUS WIDTHS

It is measured that the energy over head required for various FPF CODEC designs proposed by different authors. They require approximately 50% energy over head for achieving FPF transitions. It is also measured that the energy over head for Bus Inver method proposed by Rstan and Burelson (1995) and Sequence Switch Coding (SSC) proposed by authors Myungchul Yoon *et al*. (2004). Compared the efficiency of these techniques with FPF CODEC designs.

Table 1 shows the energy overhead required for CODEC of various techniques.

Table 1: Shows the Energy Overhead Required for CODEC

Technique	Percentage of extra wires required for CODEC at			
	4 bit	8 bit	16 bit	32 bit
BI [10]	23.2%	12.8%	11.67%	11.27%
SSC [11]	26.4%	14.58%	15.58%	16.50%
FPF-CAC[9]	26.8%	39.16%	45.65%	48.87%

As the Bus partitioned approach is adapted for the bus invert and SSC techniques, one extra wire for each sub bus for higher (bus widths > 8 bit) is required. Our simulation results show that the FPF-CAC technique possesses additional energy reduction than Bus Invert technique and SSC techniques.

The efficiency of the FPF-CAC technique in reducing the average crosstalk delay is higher than that in any other coding scheme. However, the energy overhead for FPF-CAC technique is more and it requires almost 50% additional energy overhead for CODEC.

CONCLUSION

When wiring space is taken as a resource budget, an encoding method using more wires will have a smaller wire spacing or width. It thus presents more coupling capacitance or resistance on wire so that its capability of coupling reduction is greatly hampered. Therefore, it may not be superior to an encoding method with fewer extra wires or even to an un-coded bus. We suggest that the FPF-CAC technique is more expansive, if the area is taken into account. The Bus Invert

method is most suitable technique for achieving minimization of crosstalk in VLSI circuits, if the area is taken into account. Our study shows that bus encoding methods including those using more redundant wires for crosstalk avoidance are not viable for an on-chip bus with a 0.18 um process technology from all perspectives

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