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Research Paper

LOW POWER BUS CODING TECHNIQUE FOR MINIMIZING CAPACITIVE CROSSTALK IN DSM TECHNOLOGY

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Now a day's VLSI has become the backbone of all types of designs. Interconnect plays an increasing role in determining the total chip area, delay and power dissipation. In deep sub micrometer designs the interconnect delay plays a vital role in limiting the circuit performance. The same is also limited by crosstalk in an on-chip bus and is highly dependent on the data patterns transmitted on the bus. The cross talk is dependent on the data transition patterns on the bus. The data patterns can be classified based on the severity of the crosstalk they impose on the bus. Every 10 °C increase in operating temperature roughly doubles a component's failure rate. In this context, peak power for maximum possible power dissipation is a critical design factor as it determines the thermal and electrical limits of designs, impacts the system cost, size and weight, dictates specific battery type, component and system packaging and heat sinks, and aggravates the resistive and inductive voltage drop problems. It is therefore essential to have the peak power under control. With the proposed technique the delay has been reduced with reference to coded and un-coded bus for different widths. The simulation results shows that the power dissipation in a bus is reduced about 34% with the proposed bus encoding technique in this paper.

Keywords: VLSI, Deep sub-micrometer, CODEC

INTRODUCTION

Power dissipation in CMOS circuits is caused by three sources: (1) the leakage current which is primarily determined by the fabrication technology, it consists of reverse bias current in the parasitic diodes formed between source and drain diffusions and the bulk region in a MOS transistor as well as the sub threshold current that arises from the inversion charge that exists at the gate voltages below the threshold voltage. (2) The short circuit current (rush-through) which is due to the DC path between the supply rails during output transitions; and (3) the charging and discharging of capacitive loads during logic changes. The short circuit and leakage currents in CMOS circuits can be made small with proper

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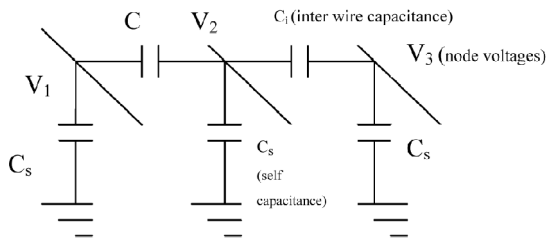
circuit and device design techniques. The dominant source of power dissipation is thus the charging and discharging of the node capacitances, which is also referred to as the dynamic power dissipation.

INTERCONNECTS IN DSM TECHNOLOGY

In DSM Technology the wires (bus lines) are called interconnects. Interconnects are used to provide connections between gates and as power supply rails or to link transistors together. A 3-bit deep sub micron model is shown in Figure 1 (Sotiriadis and Anantha Chandrakasan, 2001 and 2003;Sotiriadis, 2002). In this model C_s represents self-capacitance, C_c represents coupling capacitance. With the technology scaling, the transistor density increased tremendously and more levels of interconnects are needed. Finally the bus interconnects are heavily loaded and dissipates large amount of power.

Figure 1: Three Adjacent Wires in DSM Technology



The average power dissipation on the bus is given by

$$P_{ave} = 1/2 \times (\alpha_c C_s + \alpha_c C_c) f_{clk} V_{DD}^2 \quad ...(1)$$

And average power consumption on the bus is given by

$$P_{con} = (\alpha_c C_s + \alpha_c C_c) f_{clk} V_{DD}^2 \quad ...(2)$$

Power consumption on a bus takes place only during the transitions from 0 to 1 at the output, where as power dissipation on a bus occurs in both transitions, i.e., from 0 to 1 and 1 to 0.

It is well-known that the dynamic power dissipation in CMOS VLSI circuits is given by

$$P_{dynamic} = \Sigma C_{load} f_{clk} (V_{dd})^2 \alpha \quad ...(3)$$

where C_{load} is the total load capacitance attached to a bus line, V_{dd} is the voltage swing at operation; f_{clk} is the clock frequency and α is the switching factor. Switching activity factor α is related to the self capacitance, coupling capacitance and their switching activities.

QUADRATIC RELATIONSHIP TO POWER, VOLTAGE AND SWITCHING ACTIVITY REDUCTION

Optimizing for power entails an attempt to reduce one or more of these factors. Because of its quadratic relationship to power, voltage reduction offers the most effective means of minimizing power consumption. Without requiring any special circuits or technologies, a factor of two reductions in supply voltage yields a decrease by a factor of four in power consumption.

Dynamic power consumption depends linearly on the physical capacitance being switched. So, in addition to operating at low voltages, minimizing capacitances offers another technique for minimizing power consumption. In addition to voltage and physical capacitance, switching activity also influences dynamic power consumption. A chip may contain an enormous amount of physical capacitance, but if there is no switching in the circuit, then no dynamic power will be consumed. The data activity determines how often this switching occurs. In the past, the

major concerns of the VLSI designer were area, performance, cost and reliability; power consideration was mostly of only secondary importance. In recent years, however, this has begun to change and, increasingly, power is being given comparable weight to area and speed considerations. From the environmental viewpoint, the smaller the power dissipation of electronic systems, the lower the heat pumped into the rooms, the lower the electricity consumed and hence lower the impact on global environment, the less the office noise (e.g., due to elimination of a fan from the desktop), and the less stringent the environment/office power delivery or heat removal requirements.

The design for low power problem cannot be achieved without accurate power prediction and optimization tools or without power efficient gate and module libraries. Therefore, there is a critical need for CAD tools to estimate power dissipation during the design process to meet the power budget without having to go through a costly redesign effort and enable efficient design and characterization of the design libraries. However, it is clearly infeasible to estimate the power by exhaustive simulation of the circuit. Recent techniques overcome this difficulty by using probabilities that describe the set of possible logic values at the circuit inputs and developing mechanisms to calculate these probabilities for gates inside the circuit.

ANALYTICAL MODEL FOR COMPUTING POWER DISSIPATION AND CROSSTALK DELAY

The analytical model for computing energy and delay has been proposed by the authors Sotiriadis and Anantha Chandrakasan in (2001). The research work done previously on reducing bus energy consumption has also used the same analytical energy model. The research work done previously on reducing bus energy consumption has also used the same analytical energy model.

Consider three adjacent interconnect wires in DSM technology.

ANALYTICAL ENERGY MODEL

Analytical energy model is described by the following Equations (4) and (5). Total energy consumed during the transition is given by the sum of energy due to the self-capacitance and coupling capacitance switching.

$$E = \sum_{r=1}^{n} E_r = \sum_{r=1}^{n} E_r^L + \lambda \sum_{j=1}^{n-1} E_i^I \qquad ...(4)$$

where $E_r^L = C_L V_j^f [V_j^f - V_j^i]$ is the energy due to the self-capacitance and

$$E_j^I = C_L [(V_{j+1}^f - V_j^f)^2 + (V_{j+1}^f - V_j^i).(V_j^i - V_{j+1}^i)] \qquad ...(5)$$

It is the energy due to the coupling-capacitance. V_j^f and V_j^i are the final and initial values of the j^{th} interconnect and V_{j+1}^f is the final value of the $(j + 1)^{th}$ interconnect and λ is technology parameter and is given by $\lambda = Cc/Cs$; where Cc is the coupling capacitance and *Cs* is the substrate capacitance. The relation between these capacitances is interesting as the CMOS processes shrink, the ratio of the inter-wire capacitances (Cc) to the wire-to-ground capacitances (Cs) grows, and in modern processes the inter-wire capacitances (between adjacent wires) can no longer be disregarded. For 180 nm, 90 nm CMOS technology λ is 3.2 and 5.8, respectively. Energy dissipated by the self and coupling capacitances can also be reduced by bus coding techniques. Actually,

effective transition reduction may not always reduce the energy dissipation.

PREVIOUS WORKS ON BUS MINIMIZING THE SWITCHING ACTIVITY

As the switching activity of coupling capacitance becomes predominant in DSM technology, many number of bus encoding techniques have been proposed to reduce the switching activity of the coupling capacitance. Because, the coupling capacitance creates crosstalk related delay and energy consumption in DSM buses. Previously, so many techniques have been developed to reduce the bus transitions. The Bus Invert technique (BI) (Rstan and Burelson, 1995) is one of the most popular coding techniques. In the BI coding, if the Hamming distance between the present data and the last data of the bus is lager than N/2, the present data is transmitted with each bit inverted. An extra bit, called invert line, is required to signal the receiver side whether the bus is inverted or not. The authors Yan Zhang *et al.* (2002) (OEBI) Naveen K. Samala *et al.* (2004) (NDSB) propose different techniques by inverting odd and even lines to minimize the coupling energy. All the above techniques require two extra lines for sending control information. Another author, Khan *et al*. (2006) introduced different techniques to eliminate the class 4 and 6 cross talk in a 4 bit bus and extended the same work to 8 bit, 16 bit and 32 bit data, but bus width must be extended to 13 bit, 25 bit, and 55 bits respectively. We have developed a new Bus encoding Technique and obtained better reduction in energy and delay.

PROPOSED TECHNIQUE

Algorithm:

B=Bus width,

N= Number of data items to be transmitted,

$C_1C_2(0)$=00; Case0 //direct transmission of data //

$C_1C_2(1)$ =01; Case1 / / only even items of the data inverted and transmitted //

$C_1C_2(2)$ =10; Case2 //only odd items of the data are inverted and transmitted //

$C_1C_2(3)$ =11; Case2 //all data items of the data are inverted and transmitted //

K = 2 to N;

D_1 =First data item {a_1 a_2 a_3 a_4 a_5 a_6 a_7 a_8 C_1 C_2}

D_K = Next data item

= {B_1 B_2 B_3 B_4 B_5 B_6 B_7 B_8}

OST (D_K) = Self- transitions of odd data items.

EST (D_K) = Self- transitions of even data items.

TOST (D_K) = Original ST of data D_K.

D_K^{11} = Encoded form of data D_K.

D_K^1= Inverted form of odd data items.

D_K^2= Inverted form of even data items.

D_K^3= Inverted form of all data items.

***Start**: If CT (D_K) > (B/2-1)*

begin

*If OST (D_K) ³ EST (D_K) then **//Case 2//***

D_K^{11} = $D_K^1C_1C_2$ (2)

Bus ← D_K^{11}

D_K =D_{K+1};

D_1 = D_K^{11};

If Kd" N, go to Start

*else **// Case 1//***

D_K^{11} = $D_K^2C_1C_2$ (1)

Bus ← D_K^{11}

D_K =D_{K+1};

$D_1 = D_K^{11}$;
If Kd" N, go to Start
end
else
begin
If(TOST (D_K) *>n/2)*
$D_K^{11} = D_K^3\ C_1C_2\ (3)$ // ***Case 3//***
Bus ← D_K^{11}
$D_K = D_{K+1}$;
$D_1 = D_K^{11}$;
If Kd" N, go to Start;
Else
$D_K^{11} = D_K\ C_1C_2\ (0)$ // ***Case 0//***
Bus D_K^{11}
$D_K = D_{K+1}$;
$D_1 = D_K^{11}$;
If Kd" N, go to Start;
end.

SIMULATION RESULTS

The proposed coding scheme has been implemented using Verilog and simulated using MODELSIM for 16 and 32 bit bus. It is found from our simulation results that the power saved using the proposed method is high, when compared to other methods. The simulation results show that the proposed encoding scheme reduces the Power dissipation by 34.32% along with 22.8% reduction in crosstalk delay for a deep sub-micron bus compared to the non-coded data transmission. In particular, the area over head of the proposed scheme is less than Previous Bus encoding techniques. Thus the proposed bus encoding scheme is suitable for reducing the power dissipation and cross talk delay in VLSI circuits. However, both complexity and overhead depend strongly on the particular technology, as well as the specific circuit implementation that will be used.

CONCLUSION

This paper provides an analytical study for the design and evaluation of bus encoding schemes that can be used for on chip bus power reduction.

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