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Research Paper

SINGLE POWER CONVERSION AC-DC CONVERTER WITH HIGH POWER FACTOR AND HIGH EFFIENCY

S Manivel[1], G Ranjithkumar[1]* and S Tamileniyan[1]

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This paper proposes a single power-conversion ac-dc converter with high power factor and high efficiency. The proposed converter is derived by integrating a full-bridge diode rectifier and a series-resonant active-clamp dc-dc converter. To obtain a high power factor without a power factor correction circuit, this paper proposes a novel control algorithm.The proposed converter provides single power-conversion by using the novel control algorithm for both power factor correction and output control. Also, the active-clamp circuit clamps the surge voltage of switches and recycles the energy stored in the leakage inductance of the transformer.Moreover, it provides zero-voltage turn-on switching of theswitches. Also, a series-resonant circuit of the output-voltage doublerremoves the reverse-recovery problem of the output diodes.The proposed converter provides maximum power factor 0.995and maximum efficiency of 95.1% at the full load. The operationprinciple of the converter is analyzed and verified. Experimentalresults for a 400 W ac-dc converter at a constant switching frequencyof 50 kHz are obtained to show the performance of theproposed converter.

INTRODUCTION

The ac–dc converter consists of a full bridgediode rectifier, a dc link capacitor and a high frequency dc–dc converter.These converters absorb energy from the acline only when the rectified line voltage is higher than the dclinkvoltage. Therefore, these kinds of converters have a highlydistorted input current, resulting in a large amount of harmonicsand a low power factor. To solve the harmonic pollution causedby ac–dc converters, number of power factor correction.The PFC ac–dc converter can be implemented by using twopower-processing stages. The PFC input stage is used to obtainhigh power factor while maintaining a constant dc-link voltage.Most PFC circuits employ the boost converter. Theoutput stage, which is a high frequency dc–dc converter, gives theHowever, two-stage ac–dc converters raisepower losses and the manufacturing cost, eventually reducing thesystem efficiency and the price competitiveness. In effortsto reduce the component count, the size, and the cost, a

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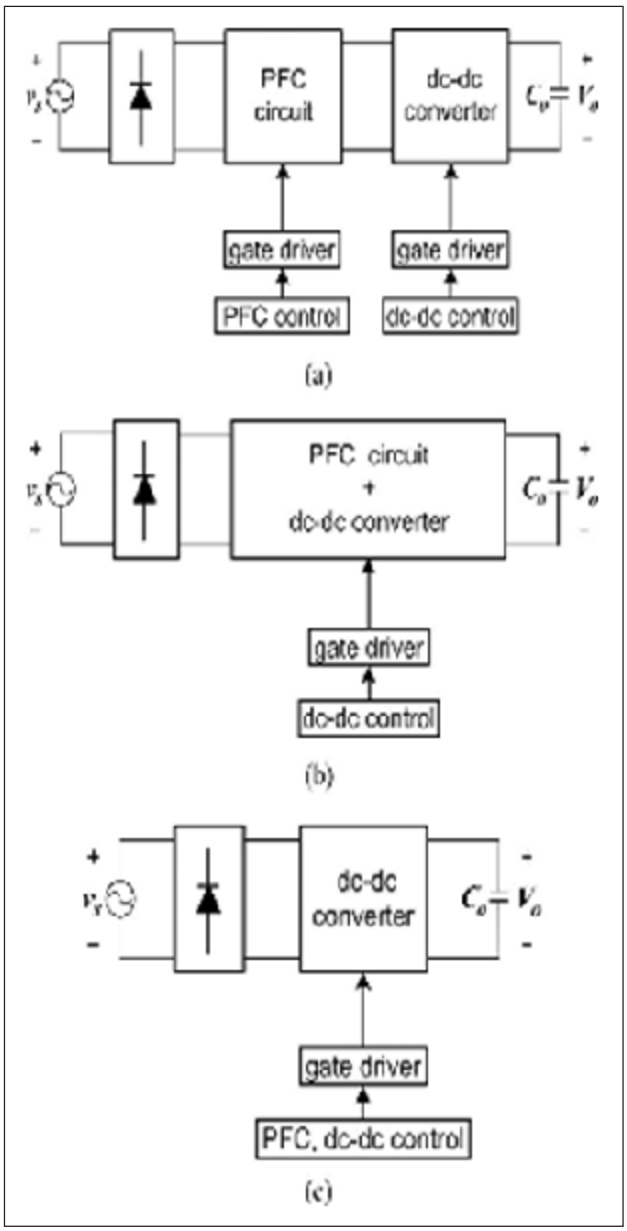
numberof single-stage ac–dc converters have been proposed anddeveloped. The main idea is that a PFC input stage and a highfrequency dc–dc converter are simplified by sharing commonswitches so that the PFC controller, the PFC switch, and its gatedriver can be eliminated. Most single-stage ac–dc converters inlow-power application employ single-switch dc–dc converterssuch as flyback or forward converters These convertersare simple and cost-effectiveThey have low switching losses because of thezero-voltage switching (ZVS) operation of the power switches.However, the conventional single-stage ac–dc converters have high voltage stresses or a low power factor in comparison with the two-stage ac–dc converter. Also, the PFC circuit used in the single-stage ac–dc converter requires the dc-link electrolytic capacitor and the inductor. The dc-link electrolytic capacitor and the inductor raise the size and the cost of the converter.Two-stage ac–dc converters consist of two power-processing stages with their respective control circuits. However, two-stage ac–dc converters raisepower losses and the manufacturing cost,eventually reducing the system efficiency and the price competitiveness. In efforts to reduce the component count, the size, and the cost, a number of single-stage ac–dc converters have been proposed anddeveloped. The main idea is that a PFC input stage and a high frequency dc–dc converter are simplified by sharing common switches so that the PFC controller, the PFC switch, and its gate driver can be eliminated.the forward converters are more cost efficiency two ac-dc converters raise the power losses and manufacturing cost,eventually reducing the system effciencyand the price competitiveness. They have high switching eventually reducing the system efficiency and the price competitiveness the PFC circuit.it implies the dc link capacitor is in effort to reduce the component count, the size and the cost a number removed form the cicuits.of single-stage ac–dc converters have been proposed and developed.The converters are simple and cost effective theymain idea is that a PFC input stage and a highfrequency dc-dc converter have high switching power losses. Single are simplified by sharing common switches so that the PFC controller is dc converter based on the asymmetrical plusPFC switches and its gate is to be terminated.Most single-stage ac–dc converter bandwidth modulations. Compare convential Nverter low-power application employ single-switch dc–dc converters insingle stage ac-dc converter with dc link electrolyte such as flyback or forward converters. These converters are simple and the rolytic capactior.this approach is mostly used cost-effective. However, they have highswitching power losses because of for single switching ac-dc converters its providthe hard-switching operation of the power switch.to overcome the drawback,ideas the low effciency to the light emitting ofsinglestageac–dc converters based on the asymmetrical pulsewidth modulation of the diode provides the current mode of power factor (APWM) half-bridge converter have been proposed they have switching supply is reduced by the power factor provides the zero voltage

This approach is mostly applied to single-switch PFC ac–dc converters. Compared to the conventional single-stage ac–dc converters with the dc-link electrolytic capacitor, the

The objectives of this proposed the single power conversion of ac-dc converter with high power factor and high power efficiency. It



composed of full bridge rectifier and a series resonant active clamp dc-dc converter.to obtain high power factor the without the PFC stage,novel control algorithm. The active clamp circuit clamps the surge voltage of switches and recycles the energy stored in the leakage. Moreover it provides ZVS operations of the switch

Provides ZVS operation of the switches. Also a resonant circuit of the output voltage doubler removes the reverse recovery problem of the output diode by zero current switching (ZVS) operations. Two stages ac-dc converter has tow processing stages with their respective control circuits.The boost type PFC converter used involtage contrmost PFC stages requires the link electrolytic capacitor and the inductor.PFC converter used in most PFC input stages requires the dc link electrolytic capacitorthe dc-link electrolytic capacitor and the inductor. Two control circuits, the dc-link capacitor and the inductor raise the size,weight and the cost of the converter and reduce the price competitiveness. On the other hand, the advantage is to decouplecontrol of the dc-link capacitor voltage from that of the outputvoltage and realize much tighter output control. Thereforetwostageac–dc converters are preferred option when reliability ismore important concerns than cost per unit.shows theschematic diagram of the voltage conventional single-stage ac–dc converter.It comprises a full-bridge diode rectifier, a PFC circuit, ahigh frequency dc–dc converter, and a control circuit for output control The PFC circuit and the high frequency dc–dc converter are simplified by sharing common switches for eliminating thePFC switch and the control circuit for the PFC circuit as shown in That is, single-stage ac–dc converters have only onecontrol circuit. Thus, the output voltage.third single-stage ac–dc converters require the dc-link electrolytic capacitor and theinductor for the PFC circuit, just like two stage converters. Finally,the conventional single-stage ac–dc converters have highvoltage stresses or low power factor in comparison with twostageac–dc convertersof the single power-conversion ac–dc converter. It consists ofa full-bridge diode rectifier, a high frequency dc–dc converter,and a control circuit. That is, the single power-conversion ac–dcconverter has also one control circuit because it has no PFCcircuit.

However, it requires the control algorithm for both PFCand output control, unlike single-stage ac–dc converters. Also,it has a large ac-dc second-harmonic ripple component reflected at the output voltage in comparison with two-stage and singlestageconverters because it has no dc-link electrolytic capacitor

However, the single power-conversion ac–dc converter providesa simple structure, a low cost, and low voltage stresses becauseit has no PFC circuit composed of the inductor, power switchingdevices and the dc-link of electrolytic capacitor. Therefore, the single power-conversion ac–dc converter is preferred option when the cost per unit is more important concerns than reliability.

Provides ZVS operation of the switches. Also a resonant circuit of the output voltage doubler removes the reverse recovery problem of the output diode by zero current switching (ZVS) operations. Two stages ac-dc converter has tow processing stages with their respective control circuits.The boost type PFC converter used in most PFC stages requires the link electrolytic capacitor and the inductor.PFC converter used in most PFC input stages requires the dc link electrolytic capacitor the dc-link electrolytic capacitor and the inductor. Two conrol circuits, the dc-link capacitor and the inductor raise the size,weight and the cost of the converter and reduce the price competitivenessthe output voltage is easily regulated bya controller and the power factor is strongly influenced by thedesign of the PFC circuit. However, single-stage ac–dc convertershave several disadvantages. First, the power factor is alsorelated to the controller, indicating that the variation of the loador the input voltage will change the power width.

CHARACTERISTICS AND OPERATION PRINCIPLE OF PROPOSED AC–DC CONVERTER

Concept of the Single Power-Conversion AC–DC Converter: This shows the schematic diagram of the conventional two-stage ac–dc converter. It comprises a full-bridge diode rectifier.Proposed single power-conversion ac–dc converter and the control block diagram of the main switch $S1$, an auxiliary switch $S2$, and a clamp capacitorCc . The switch $S1$ is modulated with a duty ratio D and the switch $S2$ is complementary to $S1$ with a short dead time the active-clamp circuit serves to clamp the voltage spike across $S1$and to recycle the energy stored in the leakage inductance of thetransformer T. Also, it provides ZVS turn- of $S1$ and $S2$. The series-resonant circuit is composed.The steady-state operation of the proposed converter includessix modes in one switching period Ts . The operating modes andtheoretical waveforms of the input side and the output side are The rectified input voltageVi is $|vin| = |Vm\sin\omega t|$, where Vm is the amplitude of the inputvoltage and ω is the angular frequency of the input voltage. Priorto Mode 1, the primary current $i1$ is a negative direction and the secondary current $i2$ is zero.*Mode 1 [t0, t1]:* At the time $t0$, the voltage $vs1$ across $S1$becomes zero and $Ds1$ begins to conduct power. After the time$t0$, $S1$ is turned on. Since $i1$ started flowing through $Ds1$ before$S1$ was turned on, $S1$ achieves the ZVS turn-on.

Operation Principle of the Proposed Circuit: Shows the proposed single power-conversion ac–dc converter and the control block diagram. The high frequency dc–dc converter used in the proposed converter combines an active-clamp

circuit and a series-resonant circuit across the power transformer *T*. The active-clamp circuit is composedsince *Vi* is approximately constant for a switching period *Ts* , the magnetizing current *im* increases linearly with the following slope:

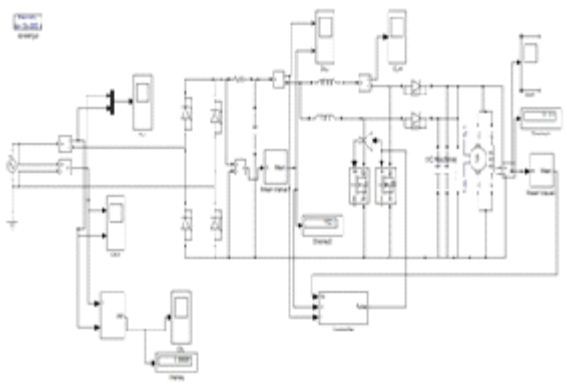
$$dm/dt=vt/Lm \quad ...(1)$$

During this interval, the input power is directly transferred to the output stage of the transformer. The difference between *i*1and *im* is reflected to the secondary current *i*2 . The secondary

$$v2 = nVi \quad ...(2)$$

where the turns ratio *n* of the transformer is given by *Ns* /*Np*. Since *Co* is sufficiently large, the resonant equivalent capacitance *Cr* is (*C*1 + *C*2). Thus, *D*1 is conducting and *Llk* resonates with *Cr* while the equations of the series-resonant circuit can be writtenas followssecondary current *i*2 flows.equations of the series-resonant circuit can be written as follows:*Mode* 2 *[t*1*, t*2 *]:* At the time *t*1*, i*1 changes its direction to positive. *Llk* and *Cr* still resonate similar to Mode1. *Mode* 3 *[t*2*, t*3 *]:* At the time *t*2*, i*2 becomes zero and *D*1 is maintained in the on-state with the zero current. *I*1 and *im*are equal during this interval. Therefore, *i*1 terminates the firstresonance andterminates the firstresonance and increases linearly as

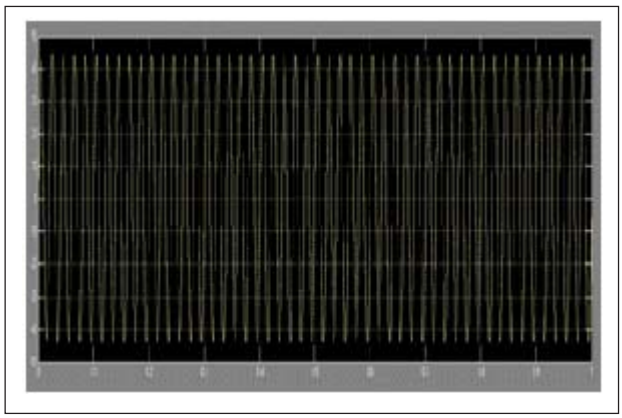
Circuit Diagram



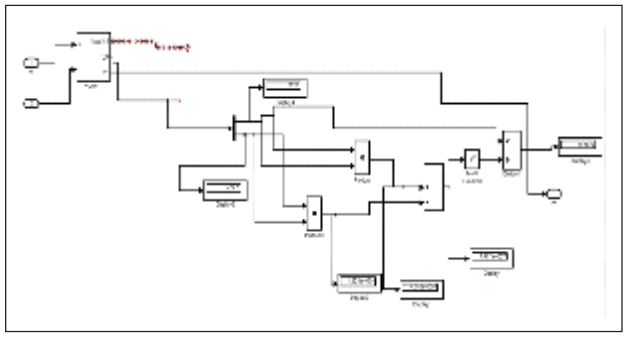
*Mode 4 [t*3*, t*4 *]:* At the time *t*3*, S*1 is turned off and *D*1 is turned off with the zero current. The ZCS turn-off of *D*1 removes its reverse-recovery problem. The voltage *vs*2 across*S*2 becomes zero and the body diode *Ds*2 begins to conductpower. After the time *t*3 , the ZVS turn-on of the auxiliary switch*S*2 is achieved. Since the clamp voltages *Vc* is approximatelyconstant during a switching period *Ts, im* decreases linearlyincreases linearly as.*Mode 4 [t*3*, t*4 *]:* At the time *t*3*, S*1 is turned off and *D*1 is turned off with the zero current. The ZCS turn-off of *D*1 removes its reverse-recovery problem. The voltage *vs*2 across*S*2 becomes zero and the body diode *Ds*2 begins to conductpower. After the time *t*3 , the ZVS turn-on of the auxiliary switch*S*2 is achieved. Since the clamp voltages *Vc* is approximatelyconstant during a switching period *TMode 1 [t*0*, t*1 *]:* At the time *t*0 , the voltage *vs*1 across *S*1becomes zero and *Ds*1 begins to conduct power. After the time*t*0*, S*1 is turned on. Since *i*1 started flowing through *Ds*1 before

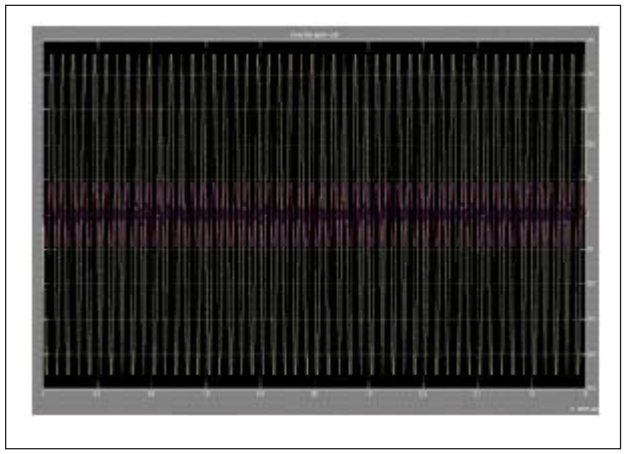
*S*1 was turned on, *S*1 achieves the ZVS turn-on.the switches *S*1 and *S*2 are ideal except for their body diodes *D*1,*D*2 and capacitances *C*1*, C*2 ; the input voltage.an ideal transformer with the magnetizing inductance *Lm* connected in parallel with the primary winding *Np* , and the leakage inductance *Llk* connected in series with the secondary winding *Ns* .Therefore, the single power-conversion ac–dc converter is preferred option when the cost per unit is more important concerns than reliability.one switching period *Ts* is much shorter than the period.the output voltage *Vo* is constant because the capacitance of the output capacitor *Co*is sufficiently large &similar The steady-state operation of the proposed converter includessix modes in one switching period *Ts* . The operating modes andtheoretical

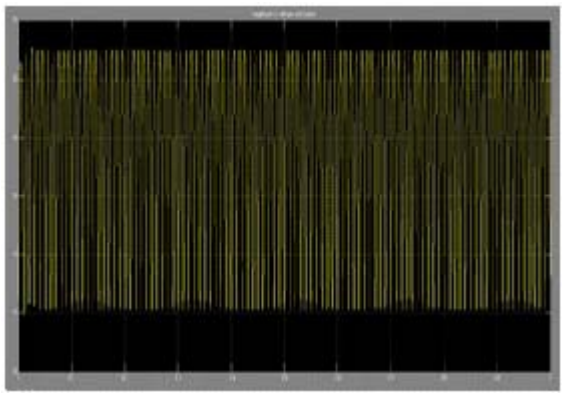
waveforms of the input side and the output side are The rectified input voltage*Vi* is |*v*in | = |*Vm*sinω*t*|, where *Vm* is the amplitude of the input voltage and ω is the angular frequency of the input voltage. Prior to Mode 1, the primary current *i*1 is a negative direction and the secondary current *i*2 is zero. The switch *S*1 is modulated with a duty ratio *D* and theswitch *S*2 is complementary to *S*1 with a short dead time. Theactive-clamp circuit serves to clamp the voltage spike across *S*1and to recycle the energy stored in the leakage inductance of thetransformer *T*. Also, it provides ZVS turn-on of *S*1 and *S*2. During this mode, the input power is transferred to the output stage like in Mode 1. The voltage across *Llk* is the difference between the secondary winding voltage *v*2 and the resonant capacitor voltage *vc*2 . Since the equivalent clamp capacitor *Cc* /*n*2 is much larger than *Cr* , the resonant effect of *Cc* is negligible in the series-resonant network that is composed of *Cc* /*n*2, *Cr* , and *Llk* . Therefore, *i*2 begins to resonate again by *Llk* and *Cr* similarto the first series resonance in Mode 1where *Vc*2 is the average voltage of *C*2. The angular resonant frequency ωr and the impedance *Zr* are equal to (6). From (9)and (12), *i*1 decreased by the second series resonance.*S*2 turn-on *V*1=*DVi*/(1 – *D*), from the volt–second balancelaw of the magnetizing inductance *Lm*, the average voltages across the resonant capacitors *C*1 and *C*2*Mode* 6 *[t*5, *t*6 *]:* At the time *t*5, *i*2 becomes zero and *D*2 is maintained to the on-state with the zero current. *i*1 and *im*are equal during this mode. Therefore, terminates the seriesresonance and decreases linearly as (9). At the end of this mode, *D*2 is turned off with the zero current. The ZCS turn-off of *D*2 removes its reverse-recovery problem.With the average voltage across the primary winding *Np*The voltage controller attempts to minimize the errorvalue as the difference between *Vo* ,ref and the measured output voltage by adjusting *i"o* , that is, *i"o* is calculated by the voltagecontroller, and then *i"o* is calculated by the PFC rule in Inorder to realize the PFC rule, synchronization with input voltage*v*in is necessary. Since *Vi* includes the information aboutthe amplitude and the phase of *v*in , the synchronization with vin implemented by using vt.*v*in is implemented by using *Vi.*



SUBSYSTEM







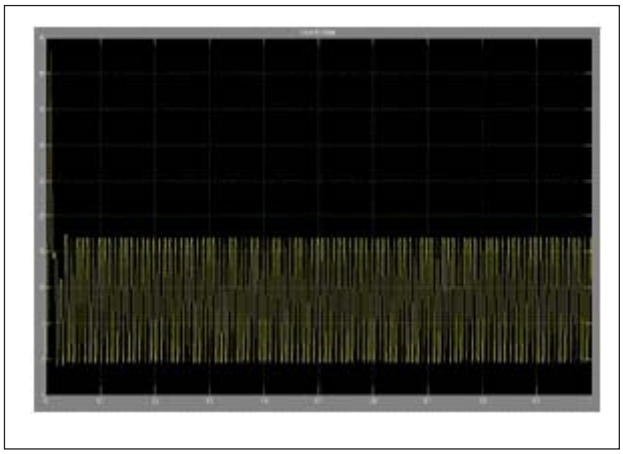
Mode 5 *[t*4*, t*5 *]:* At the time *t*4*, Llk* and *Cr* still resonatesimilar to Mode 4. In addition, *i*1 may change its directionduring this interval based on the designed resonant frequency fr.

The proposed converter has no PFC circuit. Therefore, to obtain a high power factor, it requires the control algorithm for both PFC and output control. The duty ratio *D* according to theinput current *i*in is hard to control because the relation of *D* and *i*in is nonlinear. To achieve good controllability, the nonlinear system needs to be transformed into the linear system by the feedback linearization. Δ*im* is current variations of *im* for one switching period *T*s. The ripple component of *Vc* can be neglected by the large clamp capa*D* is obtained by adding *D* to *Dn*citor value. Therefore, from the volt–second balance*i"o* is the amplitude of the desired output current,The ripple component of *Vc* can be neglected by the large no of diode and clamp capacitor value. Therefore, from the volt–second balance law of *Lm, Vc.*

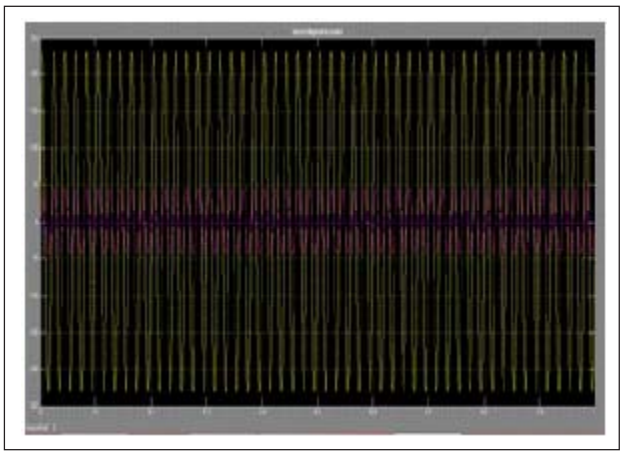
Control Algorithm: The proposed converter has no PFC circuit. Therefore, to obtain a high power factor, it requires the control algorithm for both PFC and output control. The duty ratio *D* according to the input current *i*in is hard to control because the relation of *D* and *i*in is nonlinear. To achieve good controllabil ity, the nonlinear system needs to be transformed into the linear system by the feedback linearization. Δ*im* is current variations of *im* for one switching period *Ts* . The ripple component of *Vc* can be neglected by the large clamp capacitor value. *Vi* includes the information about the amplitude and the phase of *v*in , the synchronization with *v*in is implemented by using *Vi* as shown in Fig. 2. The current controller attempts to minimize the error value as the difference between *i"o* and the measured output current *io* by adjusting Δ*D*. Finally, *D* is obtained by adding Δ*D* to *Dn*where *Hi*(*s*) and *Hv* (*s*) are current sensor gain and voltagesensor gain, respectively. The small signal transfer functions of the duty ratio-to-output current and the output current-to voltage, respectively. *Dn* is decoupled from and the relation of Δ*D* and Δ*im* is linear. Also, the rectified input current variation Δ*Ii* is equal to the primary current variation Δ*i*1 = Δ*im* because Δ*i*1 = Δ*i*2 /*n* is zero. Thus, the relation of *Ii* and *D* is linear. In conclusion, the nonlinear system becomes the firstorder linear system by controlling *D*The inner loop is the current control loop and the outer loop is the output voltage control loop. The proposed control system is analyzed by using a small signal model. The crossover frequency of the open-loop transfer function *Tv* (*s*) for the voltage controller is chosen much smaller than the open-looptransfer function *Ti*(*s*). The proportional gain *Kpc* of *Cic* (*s*) is set up to be high enough to ensure the high bandwidth and make *io* track its current reference *i"o* rapidly. The proportional gain *Kpv* of *Cvc* (*s*) isturned as small as where the variables *io* (*s*)*, vo* (*s*), and *d*(*s*) are the small signals of *io, Vo* , and *D*, respectively. The PI compensator for the outer voltage loop *Cvc* (*s*) and the P compensator for

the inner current,to be used by the dc-ac converter for their secondary current is zero according to the variation of the amplitude and the

Maximum efficiency of 95% full laod.power factor And their dc-ac converter provides the voltage for And switching their power efficiency and factor loop *Cic* (*s*) possible to have less influence on the current control loop, and the integral gain *Kiv* of *Cvc* (*s*) is designed,the stability and dynamics of the proposed converter can be analyzed.shows the bode plot of *Top* (*s*) with designed parameters. The gain and phase margins are infinite and 140.1%, respectively. The proposed converter is a highly stable system whose stability is not affected by its gain. It also possesses considerable phase margin. Hence, it is theoretically acceptable for the controller's gain to tend to infinity since overshoots or oscillations will be damped by the high phase.



Design Guidelines: The design guidelines of the proposed converter are introduced. These guidelines help to define the ac–dc converter with the input voltage *v*in. From (19), the voltages across the switches *S*1 and *S*2. if *Vi, Vo* , and *D* are selected, the voltage margin of the switches *S*1 and *S*2 can be calculated from (32).The soft switching of *S*2 is naturally achieved by the stored energy in *Llk* and *Lm*. However, the ZVS design of *S*1 is determined by *Lm* and *po*. The relationship between *Ii* and *io* has an inverse proportion with the relationship (16). Also, since the average of the secondary current is zero, the average of the magnetizing current *im,*avg is equals to *Ii* and can be obtained from the relationship between *Ii* and *io*Since *Vi* includes the information aboutthe amplitude and the phase of *v*in, the synchronization with *v*in is implemented by using *Vi* as shown in The current controller attempts to minimize the error value as the difference between *i"*where *fs* is the switching frequency. From Fig. 5, *po* ,peak is twice the rated output power *Po* because the average value of



Parameters	Symbols	Value
Input voltage	v_{in}	90~265V_{rms}
Output voltage	V_o	200V
Switching frequency	f_s	50kHz
Input capacitor	C_i	2.2μF
Clamp capacitor	C_c	2.2μF
Magnetizing inductance	L_m	435μH
Secondary leakage inductance	L_{lk}	1μH
Primary winding turns	N_p	45turns
Secondary winding turns	N_s	18turns
Resonant capacitors	C_1, C_2	2.2μF
Output capacitor	C_o	330μF
Components	**Symbols**	**Part number**
Switches	S_1, S_2	W26NM60
Transformer core	T	PQ3535
Output diodes	D_1, D_2	15ETH03
Full-bridge diode rectifier		RBV-1506

the instantaneous output power *po* is the rated output power *Po* .According to the variation of the duty ratio *D*, the critical magnetizing inductance value to satisfy the turn-on ZVS condition of the switches *o* and the measured output current by adjusting ΔD.

An experimental prototype was implemented to verify thetheoretical analysis. It was designed for the following specifications: input voltage *v*in = 90–265 Vrms, output voltage *Vo* = 200 V, rated output power *Po* = 400 W, and switching frequency *fs* = 50 kHz.

The major components and parameters of the prototype used for experiments were presented in

The turns ratio *n* of the transformer was selected as *n*

Then, the turn-on ZVS condition (36) of *S*1 and *S*2 resulted in *Lm* <460 μ H and the magnetizing input voltage *v*in = 90–265 Vrms, output voltage

Vo = 200 V, rated output power *Po* = 400 W, and switching

frequency *fs* = 50 kHz. The major components and parameters

of the prototype used for experiments were presented in Table 1.

The turns ratio *n* of the transformer was selected as *n* = 0.4.

Then, the turn-on ZVS condition (36) of *S*1 and *S*2 resulted in*Lm* <460 μH and the magnetizing inductance *Lm* was selected as 435 μH, Also, the resonant capacitors, *C*1=*C*2 = 6.6 ìF,were selected from the turn-off ZCS condition (37) of the outputdiodes *D*1 and *D*2 . The control algorithm was implementedfully in software using a single-chip microcontroller, Microchipthe resonant capacitors,*C*1=*C*2 = 6.6 μF,were selected from the turn-off ZCS condition (37) of the output

diodes *D*1 and *D*2 . The control algorithm was implemented fully in software using a single-chip microcontroller, Microchip dsPIC30F3011. shows the waveforms of the input voltage and the inputcurrent. The input current is sinusoidal and in phase with theinput voltage. The measured power factor is greater =than 0.99.the resonant capacitors, *C*1=*C*2 = 6.6 μ F, were selected from the turn-off ZCS condition (37) of the output diodes *D*1 and *D*2. The control algorithm was implementedfully in software using a single-chip microcontroller, Microchipshows the waveforms of the input voltage and the inputcurrent. The input current is sinusoidal and in phase with theinput voltage. The measured power factor is greater than 0.99.by the reverse-recovery problem are reduced.Thepower efficiency under different loads. The measured power efficiency is over 95% at full load. The efficiency is measured by the digital power meter Yokogawa WT130. The measured maximum efficiency is about 95.1% at the full load.The turns ratio *n* of the transformer was selected as *n* = 0.4.Then, the turn-on ZVS condition (36) of *S*1 a*S*2 resulted in*Lm* <460 μH and the magnetizing inductance *Lm* was selected.

CONCLUSION

Therefore, the proposed converter is suitable for low-powerapplications. The proposed converter has low line current harmonicsto comply with the IEC 61000-3-2 Class D limits andthe high power factor of 0.995 by using the proposed control algorithmfor both PFC and power control. The proposed controlalgorithm can be used to the boost type PFC ac–dc converters since it is

based on the control algorithm of the PFC boost converter in the continuous conduction mode. The proposed converter provides the high efficiency of 95.1% at the full load by the single power-processing, the turn-on ZVS mechanism of the switches by the active-clamp circuit, and the turn-off ZCS mechanism of the output diodes by the series resonance.as 435 ìH, Also, the resonant capacitors, *C*1=*C*2 = 6.6 ìF, were selected from the turn-off ZCS condition (37) of the output diodes *D*1 and *D*2 . The control algorithm was implemenfully in software using a single-chip microcontrollerds. resonant capacitors. The proposedconverter provides the high efficiency of 95.1% at the full loadby the single power-processing, the turn-on ZVS mechanism ofthe switches by the active-clamp circuit, and the turn-off ZCSmechanism of the output diodes by the series

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