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Research Paper

DESIGN AND ANALYSIS OF H-BRIDGE CASCADED ASYMENTRIC MULTILEVEL INVERTER FOR SINGLE PHASE INDUCTION MOTOR DRIVES

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In this paper, H-Bridge cascaded multilevel inverter is proposed for single phase induction motor drive. Number of output levels is increased, by using ternary mode Asymmetric Multilevel inverter. IGBT plays a major role in multilevel inverter. The total amount of harmonics distortion (THD) and electromagnetic interference are decreased by increasing number of levels. In this paper, 27 level ternary mode asymmetric multilevel inverter is used for single phase induction motor. Simulation results can be gained from Mat lab/stimulant to simulate 27 levels of voltage with only three power sources and three H-bridges.

Keywords: Cascaded H Bridge inverter, low THD, IGBT

INTRODUCTION

Now a day's industries are required high power rating applications. But, two level inverters are not applicable for high power applications. If two level inverters are used in high power applications, the power elements are damaged due to high voltage stress. So, multilevel inverter is used for industrial Applications. This inverter generates a several levels of dc voltage output mostly similar to the sine wave.

Multilevel inverter gives many advantages like low total harmonics distortion (THD) (Chunmei Feng and Vassilions G Agelidis, 2000), lower dv/dt ratio, voltage stress, high output power quality, higher efficiency, low switching frequency and low switching losses. Using multilevel configuration, the amplitude of the voltage can be increased, voltage stress in the switching components is decreased and the overall THD is reduced. It gives more advantages such as simple circuit, less number of components. A variety of topologies for multilevel inverters have been proposed over the years. Familiar ones are diode-clamped (Saeedifard M *et al*., 2009; Alepuz S *et al*., 2009; Rodriguez I *et al*., 2002; Rodriguez J; Renge M M and Suryawanshi H M, 2008), flying capacitor or multicell (Stala R *et al*., 2009; Stala R *et al*., 2009; Lezana L *et al*., 2009; Escalante M F *et al*., 2002; Huang I and Corzine K A, 2006; Peng F Z, 2001), cascaded H-bridge (Tolbert M *et al.*, 2002; Corzine K A *et al.*, 2004; Hua C C *et al.*, 2009; Cecati C *et al.*, 2010), and simplified

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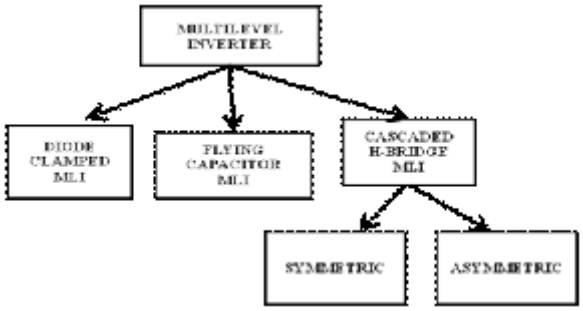
Figure 1: Types of Multilevel Inverter



H-bridge multilevel (Agelidis V G *et al*., 1997; Park S J 2003; Selvaraj J and Rahim N A, 2009; Rahim N A and Selvaraj I, 2010).This paper describes the development of a simplified H-bridge single-phase multilevel inverter.

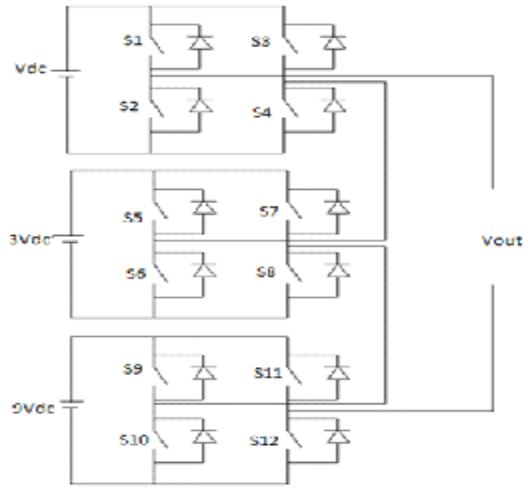
In this proposed technique to obtain a multilevel output using less number of power switches while comparing with ordinary cascaded multilevel inverter.

H-BRIDGE MULTILEVEL INVERTER

The traditional two levels or three levels inverter does not completely eliminate the harmonics in the output waveform. Therefore, using the multilevel inverter as an alternative to traditional PWM inverters is investigated. In this topology the number of phase voltage levels at the converter terminals is 2N+1, where N is the number of cells or dc link voltages. In this topology, each cell has separate dc link capacitor and the voltage across the capacitor might differ among the cells. So, each power circuit needs just one dc voltage source. The number of dc link capacitors is proportional to the number of phase voltage levels.

The cascaded MLI has three H-Bridges each has 4 power semiconductor switches and they are arranged in H-manner. In case of voltage

Figure 2: Structure of Single Phase DC-AC Three H-Bridge 27 Levels Multi Level Inverter



sources inverter, each bridges having separate dc sources and different amplitude of voltage. These supplies are fed to different Combinations of switches. The output of each bridge is fed series with Each other. In 3 H-bridges MLI, the final output can be obtained from 1st and 3rd bridges as shown in figure 2**.**

Each H-bridge cell may have positive, negative or zero voltage. Final output voltage is the sum of all H-bridge cell voltages and is symmetric with respect to neutral point. So the number of voltage levels is odd. Cascaded H-bridge multilevel inverters typically use IGBT switches. These switches have low block voltage and high switching frequency.

The cascaded multilevel inverter is classified into symmetric and asymmetric. The number of separate dc sources have equal value is called symmetric cascaded multilevel inverter (SMLI). On the other hand, the separate dc sources have a different voltage values is called asymmetric cascaded multilevel inverter (ACMLI).Asymmetric Cascaded Multilevel inverter is gives the more

Table 1: Output Levels With Different Modes Of AMLI

AMLI	No. of Bridges	No. of levels
BINARY	2	7
	3	15
	4	31
TERNARY	*2*	9
	3	27
	4	81

number of voltage levels compare to symmetric MLI at same number of voltage sources.

AMLI is classified into binary mode and ternary mode. The ternary mode operation gives more number of output levels. The comparison of binary and ternary mode output levels is shown in the following table.

Number of separate dc sources are used in **3^n** values like 1, 3, 9, 27, etc., is called **Ternary mode** operation .so, we can get more number of levels compare to the binary mode by using same number of dc sources.

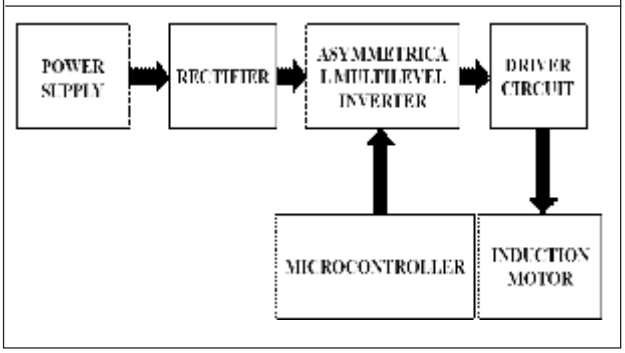
ACMLI FOR INDUCTION MOTOR DRIVE

The single phase bridge rectifier converts AC power to DC. The DC power is fed to MLI. The MLI converts the DC power to controlled AC power. The Microcontroller is used to generate the gate pulses. These gate pulses of Microcontroller are fed to the switches of MLI through the driver circuit to drive the induction motor. In the control circuit, the microcontroller can provide all essential switching pulses for power switches, results another significant drop in cost and circuit complexity.

1. Block Diagram

The single phase rectifier converts AC power into

Figure 3: Block Diagram of AMLI for Induction Motor



DC. The DC power is fed to asymmetric MLI (AMLI). The AMLI is converts the DC power into controlled AC power. The microcontroller is used to generate the gate pulse. These gate pulses of Microcontroller is fed to the switches of AMLI through the driver circuit to drive the induction motor.

WORKING OPERATION

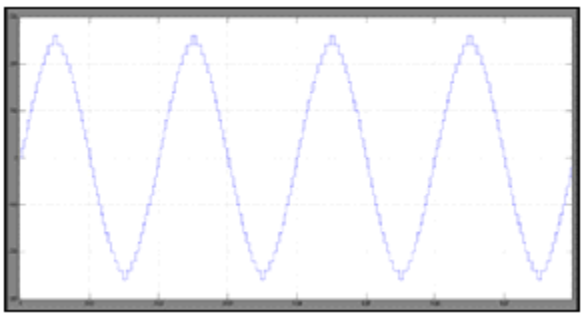
Working of proposed multilevel inverter can be easily explained in following manner.

a) Working of ACMLI

Advantage of Asymmetric CMLI is that most of the power delivered to the load by H Bridge having the highest DC source called "**MAIN**" bridge.

At full power around 81% of the real power is delivered by the Main H-bridge, 16% from the Aux-

Figure 4: Level Asymmetrical Multi Level Inverter Output



1 bridges and approximately 3% of the total power from Aux-2 bridges. All bridges have their input voltage source. They all are in the GP ratio 3. MOSFETs are used as switches. All the bridges are switching at different frequencies. The MAIN Bridge operates at fundamental frequency while the other two AUXILLARY bridges are operated at higher than fundamental frequencies.

b) Optimization Angle Control

Among other modulation, optimization angle control strategies are the most popular methods used in ACMLI because they are easily implemented in hardware. In this method for different voltage levels proper firing angles are calculated from sine equation. According to the optimized firing angles output voltages are obtained. This method is used for making hardware of asymmetrical type multi level inverter in this project. Circuits are simulated in MATLAB/ SIMULINK. In the bridge MOSFET'S are used as switches in mat lab simulink for switching the switches pulse generators are used.

EXPERIMENTAL VALIDATION

After the simulation studies, an ATMEL AT89S52 microcontroller based single-phase 27-level inverter fed 1M is fabricated and tested. The experimental validation includes the control circuit, the driver circuit and the power circuit.

1) Control Circuit

The control circuit was implemented using an ATMEL AT89S52 8-bit microcontroller. Reasons for choosing an A TMEL Microcontroller are as follows:

1) Self-sufficient standalone device (IC)

2) Cost- effective & less power consumption

Table 2: Switching States of Proposed Multilevel Inverter During Positive Half Cycle

OutputVoltage	S1	S2	S3	S4	S5	S6	S7	S8	S9	S10	S11	S12
Vdc	o	o	0	0	0	1	0	1	0	1	0	1
2Vdc	0	0	1	1	1	1	0	0	0	1	0	1
3Vdc	0	1	0	1	1	1	0	0	0	1	0	1
4Vdc	1	1	0	0	1	1	0	0	0	1	0	1
5Vdc	0	0	1	1	0	0	1	1	1	1	0	0
6Vdc	0	1	0	1	0	0	1	1	1	1	0	0
7Vdc	1	1	0	0	0	0	1	1	1	1	0	0
8Vdc	0	0	1	1	0	1	0	1	1	1	0	0
9Vdc	0	1	0	1	0	1	0	1	1	1	0	0
10Vdc	1	1	0	0	0	1	0	1	1	1	0	0
11Vdc	0	0	1	1	1	1	0	0	1	1	0	0
12Vdc	0	1	0	1	1	1	0	0	1	1	0	0
13Vdc	1	1	0	0	1	1	0	0	1	1	0	0

3) Reliability of the system

4) Software protection

5) Wide availability

The gate pulses are produced by the ATMEL AT89S52 Microcontroller. These pulses are amplified using the seven driver ICs 6N136.

2) Driver Circuit

The driver circuit describes about the isolation between the power circuit and the control circuit and the power supplied to the IGBTs. The 5V supplied by the ATMEL AT89S52 microcontroller is sensed by the buffer IC and proceeds to the IGBTs through the isolation IC 6NJ 36 which is otherwise known as optocoupler.

3) Power Circuit

A single- phase simplified nine-level inverter (SNLI) power circuit was fabricated using seven IGBT ICs CT60. The IGBT has advantages of both MOSFET and BJT, lesser power requirement and absence of secondary breakdown phenomenon.

Table 3: Ratings of Induction Motor

S. No	Parameters	Ratings
1.	Power	0.25 HP
2.	Voltage	230 V
3.	Frequency	50 Hz
4.	Speed	1500 rpm
5.	Current	2.8 A

EXPERIMENTAL RESULTS

In the capacitor -start-and -run 1M the starting winding and capacitor are permanently connected in the circuit. These motors are also known as permanent-spilt capacitor motors.

It has a comparatively low starting torque which is about 50 to 100 percent of the rated torque. The two-value capacitors run 1M motor, which start with a high value of capacitance but run with a low value of capacitance.

SIMULATIONS RESULTS

To verify the feasibility of the DER based single-phase asymmetrical 27-level inverter, a widely used software program MATLAB-Simulink is applied to simulate the circuit according to the previously mentioned operation principle. Input sources, the output voltages of each pv array are 30v, 90v, 270v respectively are connected is as shown in fig 6 to the inverter followed a linear

Figure 5: Simulation of Main Circuit

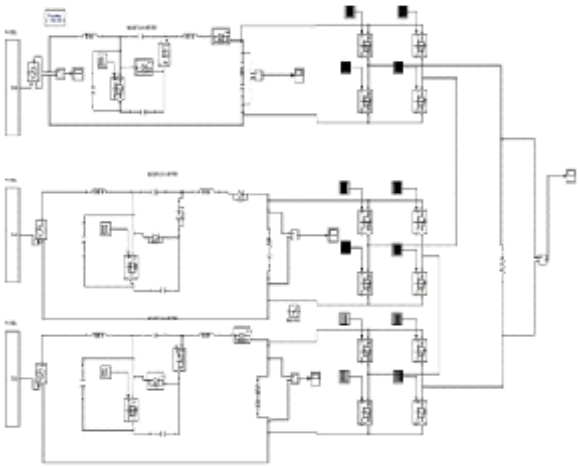
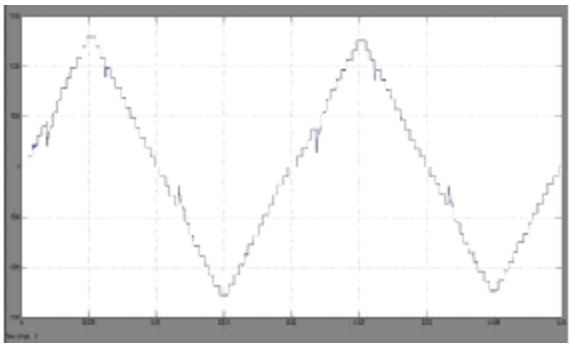


Figure 6: Twenty Seven Level Output



resistive load through the high step-up dc/dc converters. High step up converter topology in used to boost and stabilize the output dc voltage of DER such as various PV arrays for employment of the proposed simplified multilevel inverter The three input voltage sources feeding from the high step-up converter is controlled at *Vdc*1 = 100v, *Vdc2* = 3 *V*, *Vdc*3 = 9 *V* corresponding lower inverter generates a fundamental output voltage of 1280V using three individual DC sources.. Based on the simulation results, the proposed multilevel inverter was tested by a prototype. It is compared with the conventional multilevel inverters, i.e., diode-clamped, flying capacitor, cascaded H- Bridge, and cascaded transformer based multilevel inverter. In the case of diode-clamped, a large number of clamping diodes are a severe drawback and a lot of balancing capacitors is a disadvantage of the flying capacitor method. Among them, the isolated CML looks very effective to synthesize output voltage levels. It only needs a single dc input source. However, it shows low Efficiency because of adopting a cascaded transformer. And it will be suffered from large size and heavy weight. Moreover, this method is not desirable for the motor drives employing VF control scheme because of the saturation of transformer.

CONCLUSION

In this Paper much effort has been focused on the development of environmentally friendly distributed energy resources (DERs) along with cascaded H-bridge multilevel inverter employing ternary dc sources to obtain a large number of output voltage levels with minimum devices. The proposed inverter can synthesize high quality output voltage near to sinusoidal waves. The proposed prototype consists of three dc sources with the use of 12 switches Valuable and presentable merits of the proposed approach are summarized as

(1) Economical circuit configuration to produce multilevel outputs by using ternary input sources,

(2) Easy to increase of the output voltage levels and output power owing to modularity characteristic,

(3) Little transition loss of switches due to low switching frequency and reduced EMI; it is suitable for high voltage applications.

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