International Journal of Engineering Research and Science & Technology

ISSN : 2319-5991
Vol. 1, No. 2
April 2015

2nd National Conference on "Recent Advances in Science Engineering & Technologies" RASET 2015

Organized by

Department of EEE, Jay Shriram College of Technology, Tirupur, Tamil Nadu, India.

www.ijerst.com

Email: editorijerst@gmail.com or editor@ijerst.com

International Journal of Engineering Research and Science & Technology

ISSN 2319-5991 www.ijerst.com
Special Issue, Vol. 1, No. 2, April 2015
2nd National Conference on "Recent Advances in Science, Engineering&Technologies" RASET-2015

Research Paper

A NOVEL CASCADED MULTILEVEL INVERTER USING MCPWM WITH REDUCED HARMONICS

T Sankarbalaji[1]* and Dr Y V Siva Reddy[1]

*Corresponding Author: ***T Sankarbalaji*** ✉ sankarbalajieee@gmail.com

This paper deals with Single Phase Five level Inverter using Multi Carrier Based Pulse width modulation Technique. The multilevel inverter is used to improve the voltage quality by reducing the harmonics, as the number of voltage levels of multilevel inverter is increased the harmonics are reduced and hence losses are minimized significantly. We have considered the Flying Capacitor Multilevel Inverter (FCMLI), the Neutral Point Clamped or the Diode Clamped Multilevel Inverter and the Cascaded H-Bridge Multilevel Inverter. The comparison between these inverters is based on the % of THD present in the output voltage. The performance of chosen FCMLI is confirmed through MATLAB SIMULINK based simulation. It is observed that sinusoidal reference with PODPWM provides output with relatively low distortion. The simulation of single phase cascaded five level multilevel is done using Multicarrier PWM technique and compared with steps wave. Hardware module is designed for as stepped wave and multicarrier PWM signal. The outputs of both simulation and hardware are analyzed.

Keywords: Multicarrier PWM, Diode clamped multi Inverter, Multilevel Inverter, THD

INTRODUCTION

The cascaded multilevel inverter offers more than the two different voltage levels. A desired output voltages waveform can be synthesized from the number of voltage levels with low distortions, at less switching frequency, high efficiency and lower voltage rating devices. An important question in designing an effective multilevel inverter is to ensure that, the total harmonic distortion (THD) in the output voltage waveform is small. Multilevel topologies presents numerous advantage with compared to their conventional two level inverter such as high power quality waveforms, low switching losses, high voltage capability, low level electromagnetic compatibility etc. During these few decades many multi level topologies have been proposed. Contemporary research has engaged from novel inverter topology and unique modulation strategy.

Diode clamped multilevel inverter (DCMLI), Flying capacitor multilevel inverter (FCMLI), and Cascaded multilevel inverter (CMI). Most converters are chosen on the basis of components count because it directly affects

[1] PG Scholar, Dept. of ECE, Annai Mathammal Sheela Engineering College, Namakkal, India.

these cost factor and reliability. On comparing to the CMI topology with DCMLI and FCMLI shows that CMI requires less number of components and its dominant merit is circuit layouts with flexibility [2].

The PWM techniques involve the generation of a digital waveforms, for they which the duty cycle is modulated that the averages voltage of the waveform corresponds to a pure sine wave. The simplest way of producing the PWM signal is through comparison of a low-power reference sine wave with a triangle wave. Multicarrier PWM methods uses high switching frequency carrier waves in comparison to the reference waves to generate a sinusoidal output wave [3]. They offer improved output waveforms, smaller filter size, low EMI, lower total harmonic distortion (THD). Multilevel inverter topology has the least components for a given number of levels. Cascaded H-Bridge MLI topology is based on the series connection of H-bridges with separate DC sources [4].

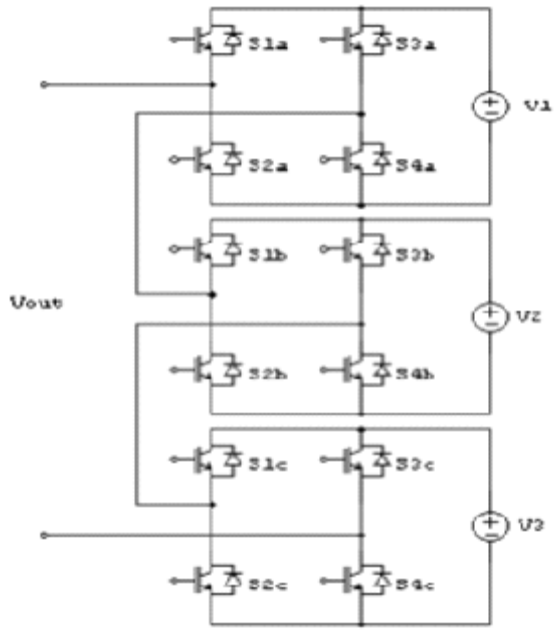
The reference waveform is compared with carrier signals and if it is greater than a carrier signal then switch/device correspond to that carrier is switched on and if the reference is less than carrier signals then device correspond to carrier is switched off [5].

Developed sinusoidal PWM of multilevel inverter in the over modulation region. This literature survey reveals few papers only on various PWM techniques and hence this work presents a novel approach for controlling the harmonics of output voltage of chosen MLI fed IM employing sinusoidal switching strategies. [6]. made a comparative study on carrier overlapping PWM strategies for five level flying capacitor inverter. Huang and Corzine [8] proposed extended operation of flying capacitor multilevel inverters. To made a survey on topologies, controls and applications in multilevel inverter [7].

EXISTING METHOD

Three phase H- bridge modules are connected to same DC source input. Single phase isolation transformers are used to isolates each H-bridge from the AC output. Primary of each transformer is connected to the each H-bridge module and secondary of the each of the transformer is connected in series to aggregates the level in the common output voltage waveforms.

Figure 1H: Bridge Multilevel Without

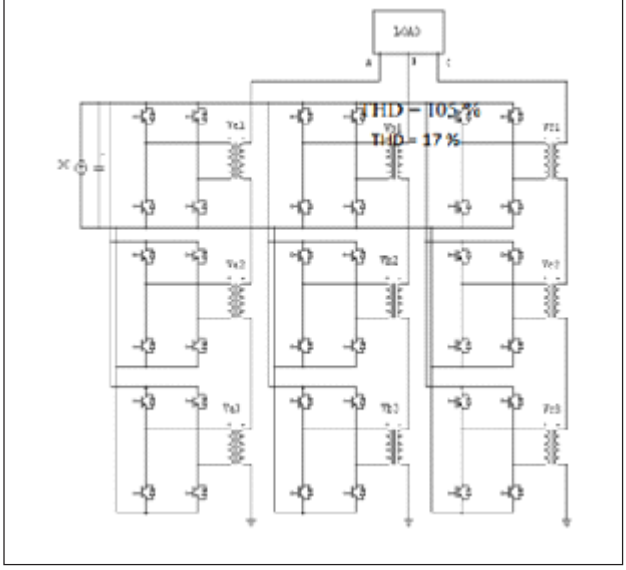


Therefore in this method configuration, the output voltages become the sum of terminal voltages of each H-bridge module. This topology presents the characteristic that the power of the DC source must be bigger than their DC sources in the conventional cascade topology, because of the high current level.

MULTILEVEL SHEPWM TECHNIQUE

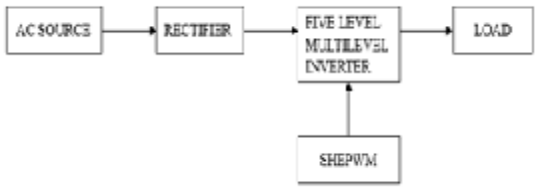
The selective harmonic elimination has a potential to achieve the high output power quality at low switching frequency in comparison with other methods.

Figure 2: Modified hybrid Multi level



The simplest way of producing the PWM signal is through comparison of a low-power reference sine wave with a triangle wave. Multicarrier PWM methods uses high switching frequency carrier waves in comparison to the reference waves to generate a sinusoidal output wave. The Figure-2 shows multicarrier PWM waveform for cascaded multilevel inverter.

Figure 3: Block Diagram of Existing System



Multilevel inverters provide more than two voltage levels. A desired output voltage waveform can be synthesized from the multiple voltage levels with less distortion, less switching frequency, higher efficiency, and lower voltage devices. The generalized multilevel inverter topology can balance each voltage level by itself regardless of inverter control and load characteristics. The existing multilevel inverters such as diode-clamped and capacitor-clamped multilevel inverters can be derived from this generalized inverter topology.

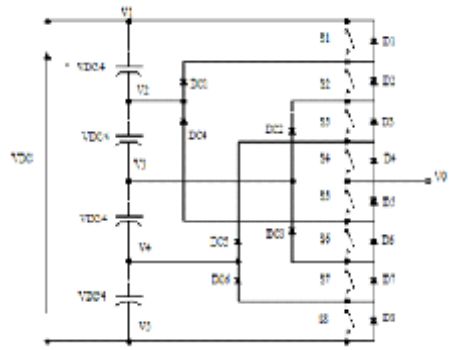
MULTI LEVEL INVERTER

The multilevel VSI is recently applied their much of industrial application such as AC power supplies, static variable compensators, drive systems, etc., One of the significant advantages of multilevel configuration is the harmonic reduction in the output waveform without increasing switching frequency of decreasing the inverter power output.

Diode Clamped Multi Inverter

The Diode-Clamped Multilevel Inverter uses capacitors in series to divide up the DC bus voltage into a set of voltage levels. To produce m level of the phase voltage, an m level diode-clamp inverter need m-1 capacitors on the DC bus.

Figure 4: Diode Clamped Multi Inverter



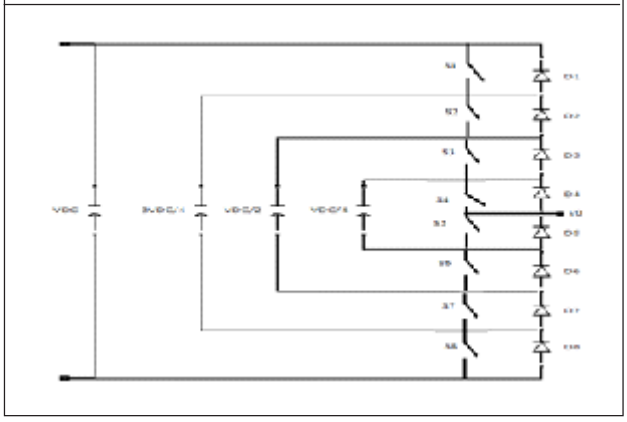
The simulation is performed for various pulse triggered flip-flops such as explicit data close to output and modified hybrid latch flip-flop design to demonstrate the effectiveness of our proposed design.

Figure 5: Switching patterns of Diode Clamped Multilevel Inverter

POWER INDEX VALUE	OUTPUT PHASE VOLTAGE(V_o)				
	V1	V2	V3	V4	V5
S1	1	0	0	0	0
S2	1	1	0	0	0
S3	1	1	1	0	0
S4	1	1	1	1	0
S5	0	1	1	1	1
S6	0	0	1	1	1
S7	0	0	0	1	1
S8	0	0	0	0	1

DIODE CLAMPED MULTI INVERTER

Figure 6: Diode Clamped Multi Inverter



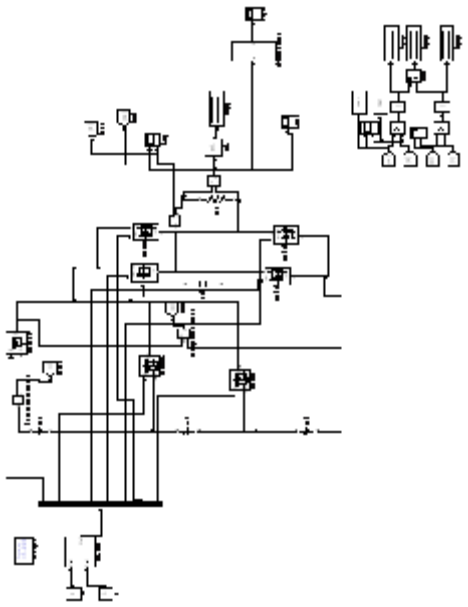
To generate m-level staircase output voltage, m1 capacitors in the D bus are needed. Each phase-leg has an identical structure. The size of the voltage increment between two capacitors determines the size of the voltage levels in the output waveform.

Figure 7: Switch State of Multi Inverter

OUTPUT V_{ab}	SWITCH STATE							
	Sa1	Sa2	S_{an1}	S_{an}	$S_{a'1}$	$S_{a'}$	$S_{a'n-1}$	$S_{a'n}$
$V_o=V_{dc}$	1	1	1	1	0	0	0	0
$V_o=3V_{dc}/4$	1	1	1	0	1	0	0	0
$V_o=V_{dc}/2$	1	1	0	0	1	1	0	0
$V_o=V_{dc}/4$	1	0	0	0	1	1	1	0
$V_o=0$	0	0	0	0	1	1	1	1

SIMULATION RESULT

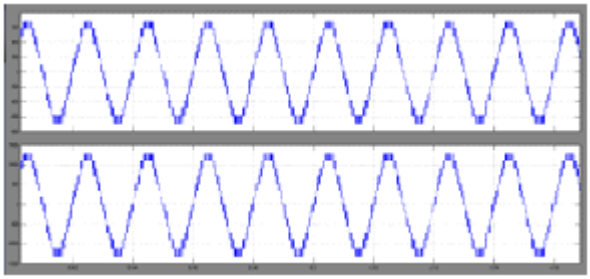
Figure 8: Simulation Result



In this symmetric multilevel inverter 12 IGBT is used. In this the diode clamped and H-bridge inverter is cascaded thus forming a hybrid topology. Basically the inverter operation is to convert the variable DC into an AC. The input dc source is given by using batteries or photo voltaic cells to the cascaded circuit. Here fuzzy logic controller is used to control the output voltage of the inverter. By using sinusoidal pulse width modulation technique the triggering pulse given to the switches are controlled.

By using the sinusoidal pulse width modulation control we can control the output by changing the magnitude and the modulation index value of the reference and carrier waveform. Mostly the carrier wave is triangular wave and the sampling wave is either we take DC signal as reference or we take sine wave.

Figure 9: Simulation Output



CONCLUSION

The cascade multilevel inverter with unequal DC sources is illustrated and the gate triggering pulse is given by microcontroller in the feedback. Here the inverter power device circuit used is MOSFET device and it has the better switching frequency and gate control compared to all other semiconductor switching devices such as SCR, TRIAC etc.,

In this 15 level asymmetric multilevel inverter output voltage is obtained using closed loop system. The future work, the number of level is increase in the cascaded multilevel inverter in order to reduce the selective harmonics elimination and to increase the voltage gain and power quality.

The output quantities like phase voltage, THD spectrum for phase voltage, and torque-speed characteristics of induction motor are obtained.

REFERENCES

1. Jae-hyun Jeon, Tae-Jin Kim, Dae-wook Kang, and Dong-seok Hyun, A Symmetric Carrier Technique of CRPWM for Voltage Balance Method of Flying Capacitor Multi-level Inverter, IEEE Transactions on Industrial Electronics, Vol.52 , No. 3, June 2005, pp. 2759-2763.
2. Boora A A, A Nami, F Zare, A Ghosh and F Blaabjerg (2010), "Voltage-Sharing Converter to Supply Single-Phase Asymmetrical Four-Level Diode-Clamped Inverter With High Power Factor Loads", IEEE Transactions on Power Electronics, Vol. 25, No. 10, pp. 2507-2520.
3. Panagis P, F Stergiopoulos, P Marabeas and S Manias (2008), "Comparison of State of the Art Multilevel Inverters", *Procs IEEE Conference on Power Electronics Specialists Conference 2008*, pp. 4296-4301.
4. Tolbert L M, J N Chiasson, Z Du and K J McKenzie (2005), "Elimination of Harmonics in a Multilevel Converter with Nonequal DC Sources", *IEEE Transactions on Industry Applications*, Vol. 41, No. 1, January/ February, pp. 75-81.
5. Nami A, F Zare, A Ghosh and F Blaabjerg (2011), "A Hybrid Cascade Converter Topology With Series-Connected Symmetrical and Asymmetrical Diode-Clamped H-Bridge Cells", *IEEE Transactions on Power Electronics*, Vol. 26, No.1, 2011, pp. 51-65.
6. Shanthi B and S P Natarajan (2010), "Comparative Study on Carrier Overlapping PWM Strategies for Five Level Flying Capacitor Inverter", *International Journal of Science and Techniques of Automatic*

control & Computer Engineering, *IJ-STA*, Vol.4, No.1, pp. 1158-1173.

7. Porselvi T and R Muthu (2011), "Comparison of Cascaded H-Bridge, Neutral Point Clamped and Flying Capacitor Multilevel Inverters Using Multicarrier PWM", *Proc. IEEE Conference (INDICON)*, pp. 1-4.
8. Haiwen L, Tolbert L M, S Khomfoi, B Ozpineci and D Zhong (2008), "Hybrid Cascaded Multilevel Inverter with PWM Control Method", *Proc. Power Electronics Specialists Conference*, pp.1- 5.
9. Ramani K (2010), "Switching Pattern Selection Scheme Based 11 levels Flying Capacitor Multilevel Inverter fed Induction Motor", *European Journal of Scientific Research*, Vol. 48,No. 1, pp. 51-62.
10. Shukla A, A Ghosh and A Josh (2004), "Flying Capacitor Multilevel Inverter and its Applications in Series Compensation of Transmission Lines", *Proc. IEEE Power Engineering Society General Meeting*, Vol.2, pp. 1453 -1458.

International Journal of Engineering Research and Science & Technology
Hyderabad, INDIA. Ph: +91-09441351700, 09059645577
E-mail: editorijlerst@gmail.com or editor@ijerst.com
Website: www.ijerst.com