International Journal of Engineering Research and Science & Technology

IJERST

ISSN : 2319-5991
Vol. 1, No. 1
March 2015

National Conference on "Recent Prends in Communication & Information Technologies"NCRTCIT 2015

Organized by
Dept. of ECE, Indra Ganesan College of Engg., Trichy, Tamil Nadu, India.

www.ijerst.com

Email: editorijerst@gmail.com or editor@ijerst.com

ISSN 2319-5991 www.ijerst.com
Special Issue, Vol. 1, No. 1, March 2015
National Conference on "Recent Prends in Communication & Information Technologies" NCRTCIT 2015

© 2015 IJERST. All Rights Reserved

Research Paper

OPTIMAL REPAIR RATE AND AREA REDUCTION FOR EMBEDDED MEMORIES BY USING BIRA & AMT

V Geetha[1]*, X Susan Christina[1] and X Susan Christina[1]

*Corresponding Author: V Geetha ✉ geeta93selvi@gmail.com

As the capacity and density of embedded memories have rapidly increased, the probability of memory faults will increase. That results in yield drops and quality degradation.Yield improvement of embedded memories have become very important.Yield refers to the percentage of good die on the wafer. For embedded memories Built-In-Redundancy-Analysis (BIRA)is used to achieve optimal repair rate and yield improvement. In this Project the proposed scheme generates set of test patterns with weights 0, 0.5 and 1 using an accumulator-based-3 weighttest pattern generation. In a Built-In Redundant analysis (BIRA) scheme, it performs exhaustive search to find and repair the faults in RAM. It uses part of spare memory as an AMT(Address Mapping Table) to reduce the faulty cell address to its logical address which consumes less area. And by using tiling technique in spare memory permanent faults were handled. These reduced addresses are stored in CAM (Content Addressable Memory) which is used during the Redundant Analysis procedure.

Keywords: Addressable Memory (CAM),Built in redundancy analysis(BIRA),Built in self test(BIST),Accumulator based 3-weighted test pattern generation.

INTRODUCTION

In modern system-on-chip (SOC) designs, embedded memories occupy a significant portion of the chiparea. Embedded memory plays a vital role in manyelectronic devices such as set-top boxes, sensors, industrialmeters and mobile phones due to its small size. Embeddedmemory mainly focuses on the reliability rather than largesize, so it is tested for faults using BIST.As the capacity anddensity of semiconductor memories have rapidly increasedwith the technological development of semiconductor manufacturing, the probability of memory faults has increased. This causes yield drops and quality degradation..As the chip area increases yield is reduced. In order toimprove the yield, testing is done by the embedded system.Circuit manufacturer must thoroughly test their productsbefore delivering them to the customers. Built-inRedundancy-repair (BISR) techniques are one main yieldenhancementtechnique for embedded RAMs with redundancy.

[1] M.I.E.T Engineering College , Trichy, Tamilnadu, India

Embedded memory is tested by using a built-in self-test(BIST) module or external automatic test equipment (ATE)before RA is performed. According to the testing method,there are two methods to repair faulty memories. They areBIRA module and an external ATE.Most RA algorithms have been based on 2-D redundantcells since the 1980s. Furthermore, various RA algorithmsfor 2-D redundancy have been developed. They are Repairmost(RM), CRESTA, LRM, and ESP are the most wellknownRA algorithms for built-in redundancy analysis(BIRA).**RM(**Repair most**)** is a simple algorithm. It countsthe number of faults in each line and allocates the spare linesto a faulty line in descending order of the number of faults.Although its repair rate is high, it is not optimal, because anexhaustive search is not performed. **CRESTA** (Comprehensive Real-time Exhaustive SearchTest and Analysis) focuses on the optimal repair rate andfast analysis. But the hardware cost is high.**LRM**(LinearRepair Most)and ESP(Essential Spare Pivot) mainly focuson minimizing the area overhead in terms of storagerequirements with a simple RA algorithm. However, therepair rates of the two algorithms are not optimal sincefaulty information is omitted.**IS** (Intelligent Solve) and **ISF**(Intelligent Solve First) algorithms achieve both low areaoverhead and an optimal repair rate. However, the twoalgorithms take a lot of time to complete the RA in caseswith complex fault distributions.

Recently, many tree-based RA algorithms have also beenintroduced that make an effort to lessen the search space.These algorithms are based on the branch and bound (B&B)algorithm. The B&B algorithm is a simple fault-drivenapproach. To overcome the restriction of these approaches,SFCC and BRANCH analyzer were introduced.**SFCC**(Selected fault count comparison) achieves a low areaoverhead and optimal repair rate, and reduces the searchspace by building a search tree based on the line faults.**BRANCH** analyzer analyzes all nodes concurrently within abranch for combinations of 2-D spares. In order to analyzeall nodes concurrently and achieve an optimal repair rate,BRANCH analyzer and SFCC store all fault informationinto fault-storing content-addressable memories(CAMs).Most BIRA approaches require extra hardwareoverhead in order to store and analyze faults in the memory.Existing approaches do not utilize spare memories duringthe redundancy analysis (RA) procedure.Proposed system uses part of the spare memory as anAddress Mapping Table (AMT) in order to reduce the areaoverhead created by Built-In Redundancy Analysis (BIRA)scheme.

RELATED WORK

A. Fault Classification

A fault in a system is some deviation from theexpected behaviour of the system: a malfunction. Faults inembedded memory may be due to variety of factors,including hardware failure, operator (user) error. Faults canbe classified into one of three categories:

Transient Faults

These occur once and then disappear. For example, anetwork message doesn't reach its destination but does whenthe message is retransmitted.

Intermittent faults

Intermittent faults are characterized by a fault occurring,then vanishing again, then reoccurring, then vanishing.These can be the most annoying of component faults. Aloose connection is an example of this kind of fault.

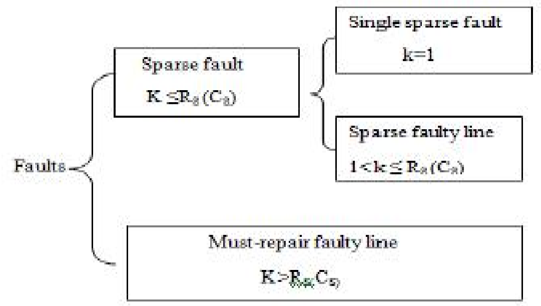
Permanent Faults

This type of failure is continues to exist until the faultycomponent is repaired or replaced. Examples of this fault aredisk head crashes, software bugs, and burnt-out powersupplies.

The **failure pattern** is classified into six types: word linefault, bit line fault, cluster fault, continuous fault, twin fault,and single fault. Word (bit) line fault is column (row)failures. Cluster fault is formed of various shapes bydistribution of faulty cells. Continuous fault is a line faultwhich has greater than two faults, i.e., faulty cells arecontinuously distributed. Twin fault is formed by a line faultor a diagonal fault by two faults. A single fault does notshare a row and column address with other faults.Since a memory with 2-D spare architecture is repairedby line replacement, faults (failure pattern) were classifiedinto three types:

- single fault
- sparse line fault,
- must-repair line fault.

Figure 1: Classification of Faults



Diagonal fault of twin fault and single fault can bedefined as a single fault. Sparse line fault is a faulty row orcolumn line.

The number of spare rows and columns are *Rs* and *Cs*,respectively A faulty row (column) line has more than oneand less than or equal to *Cs* (*Rs*) faults. Cluster fault,continuous fault, and line fault of twin fault can be definedas a sparse line fault. A must-repair faulty row (column) linehas greater than *Cs* (*Rs*) faults. Word line fault, bit line fault,part of cluster fault, and continuous fault can be defined asmust-repair line fault. Because the cluster faults containmany cross line faults, the cross line faults generatecomplicated cases for RA.

B. Spare Memory

Spare memory is a division of memory. Embeddedmemory is divided into two channels. The first channel ismirrored to the second channel, creating a redundant copy ofmemory. If a fault occurs within the memory of one channel,the memory controller shifts to the paired channel withoutdisruption, and the channels can re-synchronize when repairsare completed. In sparing mode, the trigger for failover is apreset threshold; when the threshold is reached, the contentis copied to its spare counterpart and it is activated for use.

C. Content Addressable Memory

CAM is designed to search its entire memory in asingle clock cycle, it is much faster than RAM in virtuallyall search applications. CAMs are widely used wherever fastparallel search operations are required. CAM is a storagearray designed to find the location of a particular storedvalue. The main difference between a Content Addressable Memory and a Random Access Memory (RAM) is that, in aRAM the user supplies the address and gets back the dataand in a CAM the user supplies the data and gets back theaddress. In BIRA the cam can be used to store the reducedaddresses given by AMT for analyzing the fault addressusing RA procedure.

Redundancy Analysis (RA)

After the fault collection, Redundancy Analysis(RA) procedure is done by the embedded system to findrepair solutions. In order to achieve an optimal repair rate, an RA algorithm, which is an exhaustive search method, isused. Optimal repair rate is the rate of occurrence of failureincidences for a repairable system. It is defined as the ratioof memories repaired by redundancy analysis to all repairable of the total tested memories.

$$\textit{Optimal repair rate} = \frac{\textit{Memories repaired by BIRA}}{\textit{All repairable memories of the total tested memories}}$$

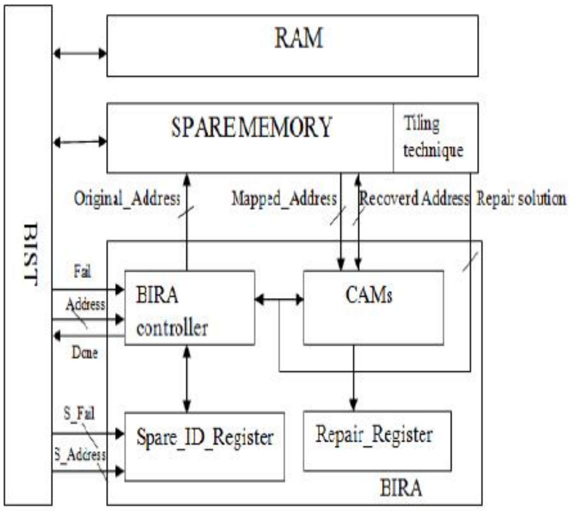
During Redundancy Analysis, all the solutioncandidates are applied to the faults according to the numberof faults. If there is one solution at least, then the memory isrepairable. If there is no solution after all the solutioncandidates are applied to the faults, then the memory isirreparable. If the number of faults is less than the sum of theavailable spare memories, there may be no solution byapplying solution candidates to the row and columncombinations of the faults.

PROPOSED WORK

The conceptual block diagram of a built-inredundancy analysis (BIRA)is shown below, which iscomposed of BIST and BIRA. Here the spare memory isused as an AMT, so it is tested by BIST before the RAM istested. This BIRA scheme has two modes, 1) Test mode 2)Normal mode.

In the test mode, BIST detects the faults in theRAM and sends the fault information to BIRA. BIRA canthen change the fault addresses into short mapped logicaladdresses. The BIST tests the RAM and the BIRAdetermines the redundancy allocation for efficientlyreplacing the defective elements of the RAM.

Figure 2: Conceptual Block Diagram of BIRA



The proposed BIRA consists of BIRA_Controller,fault storing CAMs, Spare_ ID_ register, andRepair_register. The controller performs several procedures:it compares faulty addresses, stores the original addresses inthe AMT, stores the mapped addresses in the CAMs, andrecovers the mapped addresses to the original addresses.

The mapped addresses are stored in the fault storingCAMs. The faulty addresses of the faulty spare memoriesare stored in the Spare_ID_register.The faulty spare memory is not suitable to use for theAMT as also to replace faulty memory lines.and by using thetiling technique in the spare memory the permanent faultsare handled. If detect any permanent faults in memory thetesting control avoid the prohibited zone to apply the processo it will avoids usage of the faulty zone. It will reduce theprocessing time and increases the processing speed.That is, BIRA schemes perform RA procedures takinginto account the amount of remaining good spare memory.The repair registers store the repair solutions, which are thememory addresses from the BIRA controller. Once the RAprocedure is completed, the spare memories are allocated according to the information in the Repair register.

The spare memory is tested before the RAM is tested.Because the RAM cannot be repaired by a faulty sparememory and we do not use the faulty spare memory as anAMT, the address of faulty spare memory should be storedin the Spare_ID_register. When BIST detects a fault fromthe spare memory, the signal S_Fail is asserted, and thefaulty addresses are sent to the Spare_ID_register throughthe port S_Address. The BIRA_Controller counts theavailable spare memories and checks faulty spare memory toperform an adequate RA procedure.

After the test for the spare memory is done, the RAM istested. When BIST detects a fault, it pauses and the signalFail is asserted. The faulty addresses are then sent to BIRAthrough the port Address. If the fault is the first one, theBIRA_Controller stores the fault address to the AMT byavoiding faulty spare memory in the Spare_ID_register. Otherwise, the BIRA_ Controller compares the addresseswith already stored addresses in the AMT through the portOriginal_Address.

If the address is the same, its mapped addresses are sentto the BIRA_Controller through the portMapped_Addressand are stored in the CAMs. Otherwise, the address is storedin the AMT and mapped to short logical addresses. Thesemapped addresses are sent to the BIRA_Controller through the port Mapped_ Address and stored in the CAMs. Once themapped addresses are stored in the CAMs, theBIRA_Controller asserts the signal Done, and BISTcontinues the test.

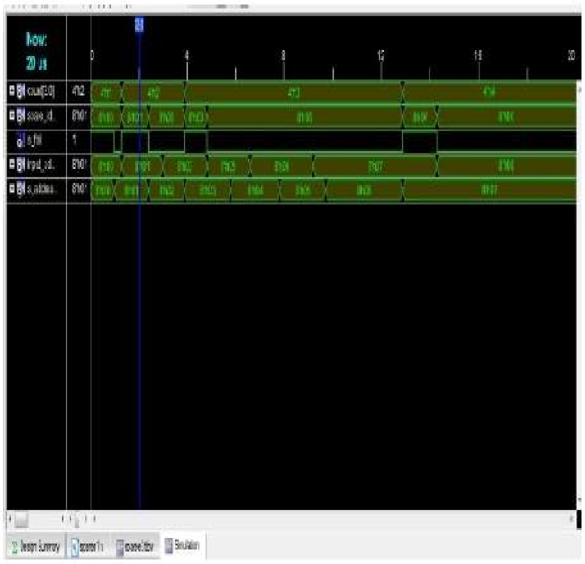
After the test is completed, BIRA finds the repair solutionby analyzing the fault information of the CAMs using theproposed RA algorithm. Because the repair solutions arecomposed of the mapped addresses, they are recovered tothe original addresses through port Recover_Address. Finally, the repair solutions, which are composed of theoriginal addresses, are stored in the Repair_register throughthe port Repair_Solution to replace the faulty lines of RAMwith spare memories.

Proposed BIRA uses the Content Addressable Memoryto store the logical address of the faulty cells in RAMmemory. When a fault is detected during the BISTprocedure, the BIRA controller stops the testing and storesthe corresponding faulty cell address in the spare memoryand it is mapped to logical address. This logical address isthen stored in CAM. When CAM receives an input faultyaddress, it searches the already stored data for match. If theincoming address is not available in its stored data, then itstores the faulty incoming address. This CAM content isused during the repairing procedure in order to recover theoriginal address.

SIMULATION RESULTS

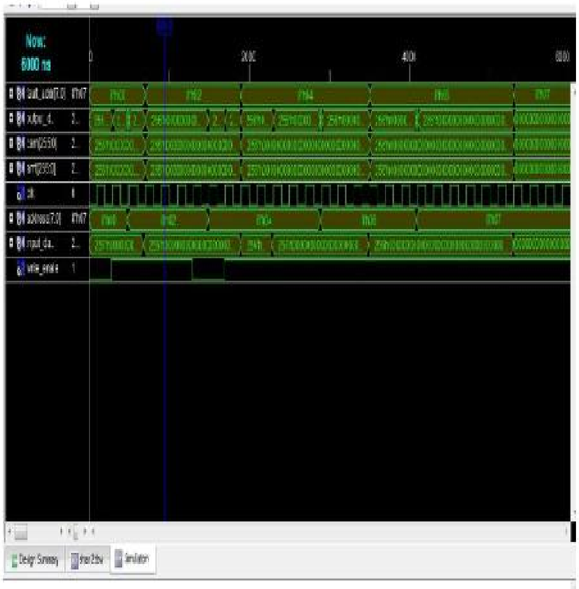
Spare memory is tested before RAM, becausefaulty spare cells cannot be used as Address Mapping Table.Input_address and the s_address are the inputs. Theinput_address and the spare cell address i.e. s_address arecompared in order to find the Address non-uniqueness typefault. If two addresses are same then it is considered as faultbecause, two cells

Figure 3: Simulation Result for Fault Detection in Sparememory



have same address i.e. address is not aunique one and it is declared as fault. Whenever a faultoccurs, the s_fail signal is asserted and the correspondingfaulty address is stored in spare_id_register. Number ofspare faults is counted by the variable count.

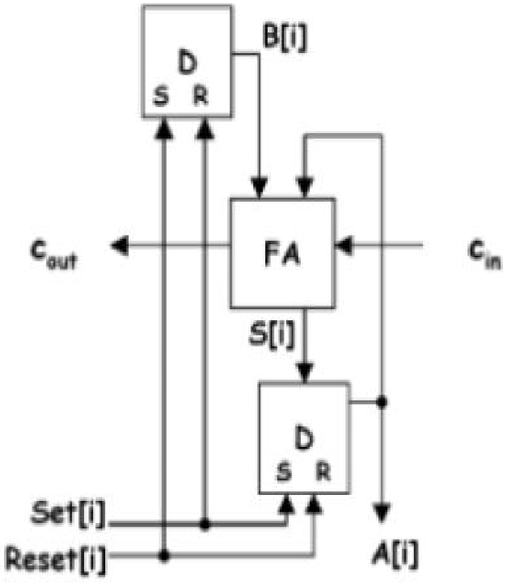
Figure 4: Simulation Result for BIRA Scheme



FURTHER IMPLEMENTATION

BIST is a design-for-testability technique thatplaces the testing functions physically with the circuit undertest (CUT).The basic BIST architecture requires the additionof three hardware blocks to a digital circuit: a test patterngenerator, a response analyzer, and a test controller. The testpattern generator generates the test patterns for the CUT. Anaccumulator-based 3-weight test pattern generation schemegenerates set of patterns with weights 0, 0.5, and 1. Sinceaccumulators are commonly found in current VLSI chips,this scheme can be efficiently utilized to drive down thehardware of built in self test pattern generation, as well.The implementation of the 3-weighted-test patterngeneration scheme is based on the full adder. Therefore, inorder to transfer the carry input to the carry output. The logicmodule provides the Set and Reset signals that drive the Sand R inputs of the Register A and Register B in-puts.

Figure 5: Accumulator cell test vector Generation Operation of the cell



I. For A[i] =1 , We give set[i]=1 and reset[i]=0 and henceA[i]=1 and B[i]=0. Then the output is equalto 1,and Cin will be equal to Co. Cin is transferred to theCout.

II. For A[i] =0 , We give set[i]=0 and reset[i]=1 and henceA[i]=0 and B[i]=1. Then the output is equalto 0, and here Cin is equal to Cout. Cin is transferred to theCout.

III. For A[i] = "-" , set[i] =0 and reset[i] =0. The D input ofthe flip-flop of register B is driven by either 1or 0,dependingon the value that will be added to the accumulator inputs inorder to generatesatisfactorily random patterns to the inputsof the CUT.

The signals that drive the S inputs of the flip-flops ofRegister A, also drive the R inputs of the flip-flops ofRegister B and vice versa. The implementation of theproposed weighted pattern generation scheme is based onthe accumulator cell is given in Figure 1, which consists of aFull Adder (FA) cell and a D-type flip-flop withasynchronous set and reset inputs whose output is alsodriven to one of the full adder inputs. This technique is usedwithout loss of generality, that the set and reset are activehigh signals. The respective cell of the driving register B[i]is also shown.

CONCLUSION

A Built-in Redundancy Analysis scheme for embeddedmemories is proposed. Fault collection in spare memoryfollowed by RAM, address mapping and repair analysis aresome of the steps in BIRA. Faults due to address nonuniquenessare considered here and fault addresses arecollected using BIRA controller. Collected faulty addressesare mapped using Address Mapping Table which resides inspare memory. Mapped faulty addresses are stored finally inContent Addressable Memory.And by using the tillingtechnique in spare memory permanent faults were handled.If detect any permanent faults in memory the testing controlavoid to apply the process to that zone. So It will reduce theprocessing time so speed will increases. An accumulatorbased 3 weighted test pattern generation will used forgenerating test sequence. It can be implemented using anyadder design and then it does not require any modification ofthe adder; hence it does not affect the operating speed of theadder. By comparing existing system this proposed systemis advanced for embedded memories.

REFERENCES

1. Chang D.M. Li J.F. and Tseng T.-Wand(2006),"A builtinredundancy-analysis scheme for RAMs with 2-Dredundancy using 1-D local bitmap," in Proc. Design,Autom. Test Eur., pp. 53–58,Mar.

2. Cho H. and Kang W. et.al(2010),"A built-in redundancyanalysis with a minimized binary search tree," ETRI J., vol.32, no. 4, pp. 638–641,Aug.

3. Chen T.-J. and Li J.-F. et.al(2012),"Cost-efficient built-inredundancy analysis with optimal repair rate for RAMs,"IEEE Trans. Comput.- Aided Design Integr. Circuits Syst.,vol. 31, no. 6, pp. 930–940,Jun.

4. Han.T,W. and Jeong et.al(2010),"An advanced BIRA formemories with an optimal repair rate and fast analysis speedusing a branch analyzer," *IEEE Trans. Comput.-AidedDDesign integr,vol 29,no 12*,pp.2014-2026,Dec.

5. Jeong W., Jin and Kang I. et.al(2009), "A Fast

Built-inRedundancy Analysis for Memories With Optimal RepairRate Using a Line-Based Search Tree",IEEE Trans VeryLarge Scale Inter (VLSI) Systems.,vol 17,no 12,pp.1665-1678,Dec.

6. Jeong W., Kang I., Jin K. and Kang S. (2009),"A fastbuilt-in redundancy analysis for memories with optimalrepair rate using a line-based search tree," IEEE Trans. VeryLarge Scale Integr. (VLSI) Syst., vol. 17, no. 12, pp. 1665–1678, Dec.

7. Joohwan Lee, Kihyun Park and Sungho Kang(2012),"High-efficiency BIRA for embedded memories with a highrepair rate and low area overhead"., Journal ofsemiconductor technology and science, vol.12, no.3, pp.515–517, sep.

8. Lee J., Park K. et.al(2009),"An area-efficient built-inredundancy analysis for embedded memories with optimalrepair rate using 2-D redundancy," in Proc. Int. SoC DesignConf., , pp. 353–356, Nov.

9. Li J.-F**,**Tseng T.W. et.al(2010)**,**"ReBISR: AReconfigurable Built-In Self-Repair Scheme for RandomAccess Memories in SOCs" ",*IEEE Trans Very Large ScaleInter (VLSI) Systems.,vol 18,no 6*,pp.921-937,Jun.

10. Pagiamtzis.K and Sheikholeslami A.(2006),"Contentaddressablememory (CAM) circuits and architecture: Atutorial and survey," IEEE J. Solid-State Circuits, vol. 41,no. 3, pp. 712–727, May.

11. Wooheon Kang, Hyungjun Cho, Joohwan Lee, andSungho Kang, Member, IEEE ., "A BIRA for MemoriesWith an Optimal Repair Rate Using Spare Memories forArea Reduction"., *IEEE transactions on very large scaleintegration (vlsi) systems*, vol. 22 pp. 2336-2349 October2013

International Journal of Engineering Research and Science & Technology
Hyderabad, INDIA. Ph: +91-09441351700, 09059645577
E-mail: editorijlerst@gmail.com or editor@ijerst.com
Website: www.ijerst.com

ISSN 2319-5991
01
9 772319 599001