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Research Paper

IMPLEMENTATION OF SYNCHRONOUSETHERNET IN TELECOMMUNICATION SYSTEM

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Accurate timing transfer and recovery over packet networks (IP, Ethernet, MPLS, etc.)has become an important requirement for delivering many telecommunication services. This requirement stems from the fact that current networks are migrating from time-division multiplexing (TDM) technologies to packet based ones, and also the need to synchronize the many timingdependent devices like TDM access devices and wireless base stations. Synchronous Ethernet (Sync-E), defined by the ITU-T, has emerged as a powerful, yet simple technology, for accurate timing transfer over Ethernet networks using "TDM-like" (precisely, SDH/SONET) timing techniques. Synchronous Ethernet are designed for the transference of clock signals over the Ethernet Physical layer. Sync-E is to provide a synchronization signal over Ethernet network.

Keywords: Synchronous Ethernet, Medium access control(MAC), WISHBONE interface, MIIM, clock synchronization, timing and synchronization

INTRODUCTION

TELECOMMUNICATION (telecom) carriers and network service providers are designing the next-generation IP based networks to meet the demand for more bandwidth, faster and more reliable services. Ethernet (IEEE 802.3) has emerged as the transport medium of choice for the packet based networking. In general, Ethernet, and complementary technologies like IP and MPLS have gained industry-wide acceptance for deployment in provider network infrastructures due to enhancements in Quality of Service (QoS), Operations, Administration and Maintenance (OA&M), congestion man-agement, and resiliency. Ethernet also gives more flexibility for integrating voice, video and data services.

However, with the transition from TDM to packet technologies, telecom network timing and synchronization will need to evolve to support the emerging packet based infrastructure. A critical piece missing from a total convergence to Ethernet is the ability to provide timing natively within the packet network. This would provide Ethernet with the capability to transport timing-sensitive applications (such as transport of TDM and circuit emulation services (CES) over packet)

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as well as distribute precise frequency references.

For example, synchronization plays a crucial role in mobile backhaul networks . Mobile wireless base stations (both Frequency Division Duplexing (FDD) and Time Di-vision Duplexing (TDD) technologies) derive their carrier radio frequencies from a highly accurate reference clock to a quality level within 50 parts-per billion (ppb). In case of FDD operation, there are two carrier frequencies, one for uplink transmission and one for downlink transmission. In case of TDD operation, there is only one single carrier frequency and uplink and downlink transmissions in the cell are always separated in time. To avoid severe interference between uplink and downlink transmissions despite the fact that the two links use the same frequency, the cells in a TDD network typically use the same uplink downlink configuration together with intercell synchronization to a common time reference to align the switch-points among all the cells. This avoids interference between the two links as uplink and downlink transmissions do not occur at the same time.

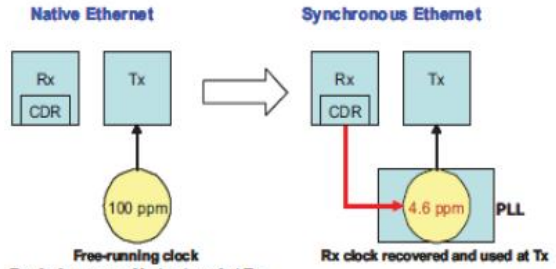
Sync-E is defined in ITU-T standards G.8261,G.8262,and G.8264.Sync-E provides Layer 1 level (physical layer) synchronization similar to PDH and SDH/SONET networks. IEEE 1588 Precision Time Protocol (PTP) provides synchronization at the Layer 2 and higher over a variety of networking technologies, while Network Time Protocol (NTP) provides synchronization over Layer 3 level with IP routed technologies.

This paper presents a discussion on the basics of Sync-E and explains how Sync-E can be supported on the existing Ethernet flavors. Ethernet provides interoperability/ interworking between all flavors but is also a technology that has a wide range of physical layer types.

RELATED WORK

Sync-E is a method of distributing frequency over Ether-net Physical Layer as defined in a *suite* of ITU-T Recommendations (G.8261, G.8262, G.8264). This method of frequency transfer is based on the well-established SONET/SDH synchronization principles widely adopted in the telecom industry. Sync-E enables the migration of carrier network from SONET/SDH-centric to Ethernet-centric infrastructure and also the interworking of SONET/SDH synchronization and Ethernet synchronization. Sync-E reuses SONET/SDH principles to allow Sync-E to interwork with SONET/SDH synchronization networks. The Sync-E specifications also en-sure interworking with native Ethernet equipment.

Figure 1: Timing in Native Ethernet versus Synchronous Ethernet



The key elements of G.8261 are as follows:

- G.8261 discusses the challenges in TDM-packet interworking, circuit emulation services (CES), and synchronization transport over packet networks as well as related issues like wander budget definition and performance

characterization in the presence of packet delay variation (PDV)

- G.8261 also describes functions that are applicable to the different modes of CES (networksynchronous solutions, and differential and adaptive methods) and provides guidance on the deployment of synchronization solutions. Sync-E passes timing directly via the physical layer interface from node to node similar to timing transfer in SONET/SDH T1/E1. Sync-E can be used in wireless backhaul to connect the wireless base stations to the mobile switching centers.

The key elements of G.8262 are as follows:

- G.8262 defines the performance characteristics of EECs. G.8262 specifies the clocks for Synchronous Ethernet equipment to ensure that Synchronous Ethernet clocks are compatible with SONET/SDH clocks as defined in G.813 and G.8162.
- G.8262 specifies clock parameters compatible with G.813: The recommendation defines requirements for clock accuracy, noise transfer, holdover performance, noise tolerance, and noise.G.8262 ensures full compatibility with the G.803 SDH reference chain.

The key elements of G.8264 are as follows:

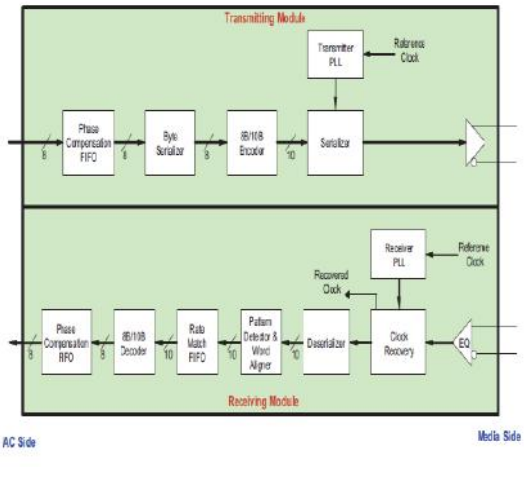
- G.8264 defines frequency transfer using Sync-E: It provides general information in addition to the operational modes (synchronous and nonsynchronous).
- G.8264 defines the Synchronization Status Message (SSM) protocol and formats for Sync-E. G.8264 also contains the specification of a synchronization signaling channel called the Ethernet Synchronization Messaging Channel (ESMC). .

ATTRIBUTES OF 100 MB/S, 1000MB/S, AND 10 IGABIT ETHERNET THAT FAVOR THEIR USE IN SYNC-E

We discuss in this section the main features of the 100 Mb/s, 1000 Mb/s, and 10 Gb/s Ethernet technologies that make them suitable for use in Sync-E. As we will see below, 10 Mb/s Ethernet PHYs cannot be used in Sync-E, and 1000BASE-T and 10GBASE-T PHYs will require special architectural handling when used in Sync- E. Our discussion focuses, in particular, on the relevant Physical Layer (PHY) features of the most commonly used Ethernet versions that are important to timing distribution.

The 100BASE-X MAC (as in all IEEE 802.3 MACs) handles the high level portions of the Ethernet protocol (framing, error detection, when to transmit, etc) and the PHY handles the low level logic (4B/5B encoding/decoding, SERDES (serialization/deserialization), and NRZI encoding/ decoding where the PHY takes a nibble (4-bits) from the MII (Medium Independent Interface) and converts this to a 5-bit binary symbol [1]. For

Figure 2: 1000BASE-X transceiver Block Diagram



100BASE-FX, this 5-bit symbol is transmitted serially on the medium. Since all data is transmitted over a single fiber, the full data rate of 100 Mb/s is present, with a frequency of 125 MHz due to the 4B/5B code conversion. However, for 100BASE-TX, RFI/EMI effects from the higher 100 Mb/s data rates on the UTP (unshielded twisted pair) are unacceptably high, so additional processing steps are required to reduce the spectral content of the transmission.

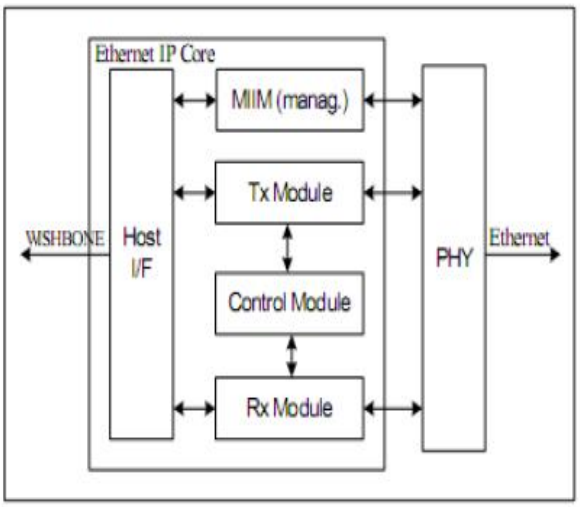
CONCEPT OF SYNCHRONOUS ETHERNET

The aim of Synchronous Ethernet is to provide a synchronization signal to those network resources that may eventually require such a type of signal. The Synchronous Ethernet signal transmitted over the Ethernet physical layer should be traceable to an external clock, ideally a master and unique clock for the whole network. Applications include cellular networks, access technologies such as Ethernet passive optical network, and applications such as IPTV or VoIP. Sync-E architecture minimally requires replacement of the internal clock of the Ethernet card by a phase locked loop in order to feed the Ethernet PHY. Extension of the synchronization network to consider Ethernet as a building block (ITU-T G.8261). This enables Synchronous Ethernet network equipment to be connected to the same synchronization network as Synchronous Digital Hierarchy (SDH).

PROPOSED WORK

The proposed work is to design synchronous Ethernet. The Ethernet IP Core is a MAC (Media Access Controller). It connects to the Ethernet PHY chip on one side and to the WISHBONE SOC bus on the other. The core has been designed to offer as much flexibility as possible to all kinds of applications.

Figure 3: Ethernet IP Core Overview



ETHERNET IP CORE FEATURES

The following lists the main features of the ethernet IP core.

- Performing MAC layer functions of IEEE 802.3 and Ethernet
- Automatic 32-bit CRC generation and checking
- Delayed CRC generation
- Preamble generation and removal
- Automatically pad short frames on transmit
- Detection of too long or too short packets (length limits)
- Possible transmission of packets that are bigger than standard packets.
- Full duplex support 10 and 100 Mbps bit rates supported
- Automatic packet abortion on Excessive

deferral limit, too small interpacket gap, when enabled

- Flow control and automatic generation of control frames in full duplex mode (IEEE 802.3x)
- Collision detection and auto retransmission on collisions in half duplex mode (CSMA/CD protocol)
- Complete status for TX/RX packets
- IEEE 802.3 Media Independent Interface (MII)
- WISHBONE SoC Interconnection Rev. B2 and B3 compliant interface
- Internal RAM for holding 128 TX/RX buffer descriptors
- Interrupt generation an all events

The Ethernet MAC IP Core consists of seven main units:

WISHBONE interface,transmit module, receive module, control module, MII module, status module and register module. Many of these modules have sub-modules. Module and submodule operations are described later in this section.

WISHBONE Interface

Consists of both master and slave interfaces and connects the core to theWISHBONE bus. Master interface is used for storing the received data frames tothe memory and loading the data that needs to be sent from the memory to theEthernet core. Interface is WISHBONE Revision B.2 and B.3 compatible (selectable with a define ETH_WISHBONE_B3 in the eth_defines.v file).

Transmit Module

Performs all transmitting related operations (preamble generation, padding, CRC,etc)

Receive Module

Performs all reception related operations (preamble removal, CRC check, etc).

Control Module

Performs all flow control related operations when Ethernet is used in full duplex mode.

MII Module (Media Independent Module)

Provides a Media independent interface to the external Ethernet PHY chip.

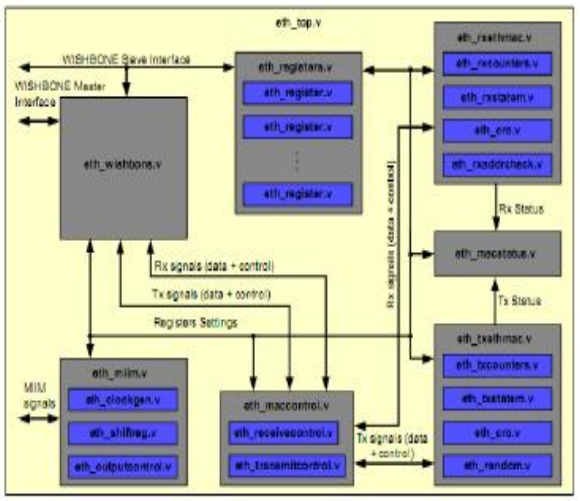
Status Module

Records different statuses that are written to the related buffer descriptors or used in some other modules.

Register Module

Registers that are used for Ethernet MAC operation are in this module.

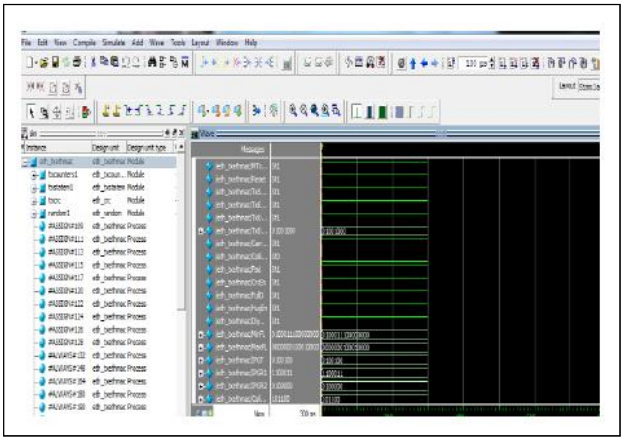
Figure 4: Ethernet Core Module



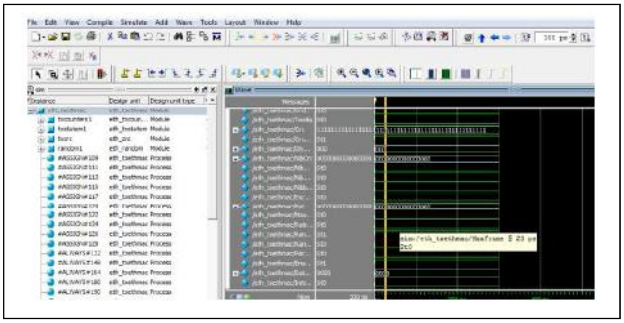
SIMULATION RESULTS

This section discuss about the simulation report and synthesis of various input and output. The following figures represent the simulation result of existing and proposed system.

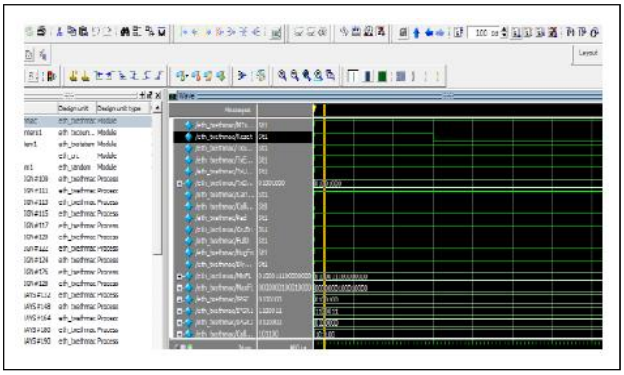
Indicates the assign of data



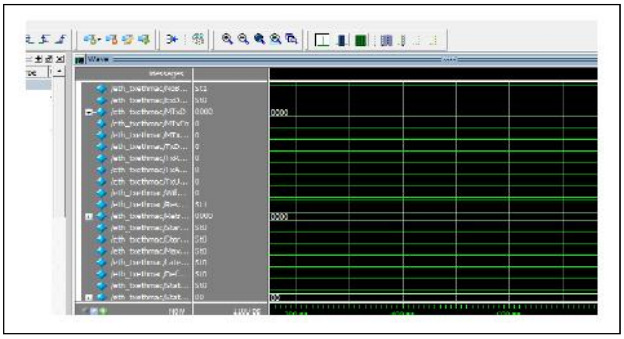
Count and check the given data



Shows the transmitted data



Shows the status of data



CONCLUSION

The Ethernet IP Core is a MAC (Media Access Controller). It connects to the Ethernet PHY chip on one side and to the WISHBONE SOC bus on the other. The core has been designed to offer as much flexibility as possible to all kinds of applications. Design of synchronous Ethernet are used for number of synchronous applications.

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