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Research Paper

FLASH STORAGE SYSTEM USING BAGC

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The Flash-based storage device is becoming a viable storage solution for mobile and desktop systems. In this paper, we propose a novel garbage collection technique, called buffer-aware garbage collection (BAGC), for flash-based storage devices. The BAGC improves the efficiency of two main steps of garbage collection, a block merge step and a victim block selection step, by taking account of the contents of a buffer cache, which is typically used to enhance I/O performance. The buffer-aware block merge (BABM) scheme eliminates unnecessary page migrations by evicting dirty data from a buffer cache during a block merge step. The bufferaware victim block selection (BAVBS) scheme, on the other hand, selects a victim block so that the benefit of the buffer-aware block merge is maximized. To identify the invalid pages and to delete the invalid pages from memory. The gated clock method is used to implemented in flash storage device.

Keywords: Flash memory, Flash Translation Layer, Buffer management layer, Garbage collection, Gate clock method

INTRODUCTION

Flash memory is an electronic non volatile computerstorage medium that can be electrically erased andreprogrammed. Flash memory stores information inan array of memory cells made from floating-gatetransistors. NAND flash has reduced erase and writetimes, and requires less chip area per cell, thusallowing greater storage density and lower cost perbit than NOR flash; it also has up to ten times theendurance of NOR flash. However, the I/O interfaceof NAND flash does not provide a random-accessexternal address bus. Rather, data must be read on ablock-wise basis, with typical block sizes of hundredsto thousands of bits. This makes NAND flash unsuitable as adrop-in replacement for program ROM, since mostmicroprocessors and microcontrollers required bytelevel random access. In this regard, NAND flash issimilar to other secondary data storage devices, suchas hard disks and optical media, and is thus verysuitable for use in mass-storage devices, suchas memory cards, Multi Media Card, Secure Digital, Memory Stick, and xD-Picture Card.

In traditional single-level cell (SLC) devices, each cell stores only one bit of information. Some

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newer flash memory, known as multi-level cell (MLC) devices, including triple-level cell (TLC) devices, can store more than one bit per cell by choosing between multiple levels of electrical charge to apply to the floating gates of its cells. The flash storage device consist of storage processor and flash chips. The main storage processor is connected to the flash chips through the flash bus and to execute the buffer management layer and Flash Translation layer. The buffer management layer manages the buffer cache in the storage device. In many flash devices, the buffer cache is usually used for write buffering because a write operation is much slower than a read operation. Thus, in this work, the buffer cache is used as a write buffer. NAND based storage such as SSD's deploy FTL, which performs an out of place update. The out of place update writes new data. Therefore the location of valid data becomes different on every update. In order to trace the physical location of data, FTL maintains the mapping table of logical sector number and its physical location. The FTL emulates the functionality of a normal block device, providing an interface between the upper layer and the flash chips.

The FTL maintains a small internal buffer for use in internal operations such as garbage collection. BAGC scheme identify the invalid page and to delete the invalid page by means of examining the contents of a buffer cache. The proposed BAGC scheme to identify the invalid page and eliminates unnecessary page migrations by means of examining the contents of a buffer cache. Our BAGC scheme consists of two techniques, the buffer-aware block merge (BABM) technique and the buffer-aware victim block selection (BAVBS) technique. BABM eliminates useless page migrations by writing up-todate pages in a buffer cache to flash memory during block merges. By doing so, BABM not only reduces the number of future page writes to flash memory, but also lowers a future block merge cost, while providing a high degree of data reliability. BAVBS chooses a victim log block to maximize the benefit of buffer-aware block merges. BAVBS exploits the locality of pages in a buffer cache for a better decision in selecting a victim block. We have evaluated the proposed BAGC scheme in the context of several state-of-the-art FTL and buffer management schemes using a trace-driven simulator.

The gated clock method is used to implemented in flash storage device. Gated clock is a method for reducing power consumption in memories. By this method the clock signal is not applied to the flip flop when the circuit is in idle condition.

RELATED WORK

There has been a considerable amount of research on a flash translation layer and a buffer management layer. Existing research on the FTL has focused on reducing the garbage collection overhead with a small mapping table. In this paper, we propose a novel garbage collection scheme, called bufferaware garbage collection (BAGC)**.**

a) Buffer Aware Garbage Collection Approach

The propose BAGC scheme identifies and eliminates unnecessary page migrations by means of examining the contents of a buffer cache. Our BAGC scheme consists of two techniques, the buffer-aware block merge (BABM) technique and the buffer-aware victim block selection (BAVBS) technique. BABM eliminates useless page migrations by writing up-todate

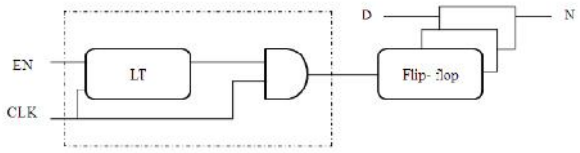
pages in a buffer cache to flash memory during block merges. By doing so, BABM not only reduces the number of future page writes to flash memory, but also lowers a future block merge cost, while providing a high degree of data reliability. BAVBS chooses a victim log block to maximize the benefit of buffer-aware block merges. BAVBS exploits the locality of pages in a buffer cache for a better decision in selecting a victim block. We have evaluated the proposed BAGC scheme in the context of several state-of-the-art FTL and buffer management schemes using a trace-driven simulator.

A synchronized enable condition allows the register bank to receive either new data from D_IN, or recycled data, depending on the condition of the enable line. But in each of these conditions, the clock continues to toggle the register every time, which dissipates dynamic power. When clock gating is added, if the enable condition is not on, then the register bank is not clocked, which saves power. The clock-gating cell is an integrated clock-gating (ICG) cell. Compared with using discrete AND gates, ICG cells save power are more area-efficient and are less likely to cause clock-skew problems. To reduce the power consumption in flash storage device.

Gated clock method

Figure 1 Shows for clock method of our target flash devices. Gated clock method used to implemented in flash storage devices. This reduces the power consumption In a digital circuit the power consumption can be accounted due to the following factors: Power consumed by combinatorial logic whose values are changing on each clock edge and Power consumed by flip-flops. Of the above two, the second one contributes to most of the power usage. A flip flop consumes power whenever the applied clock

Figure 1: Example for Gated Clock Method

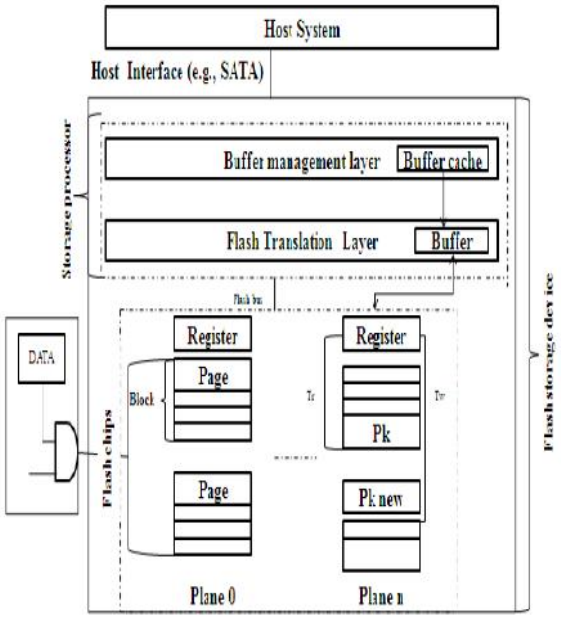


signal changes, due to the charging and discharging of the capacitor. If the frequency of the clock is high then the power consumed is also high. Gated clock is a method to reduce this frequency.

PROPOSED WORK

Figure 2 shows an architectural overview of our target flash device. Our target storage device interacts with a host system through a standard interface such as SATA (Serial Advanced Technology Attachment) and eMMC (MultiMediaCard). On the storage side, the main storage processor is connected to the flash chips

Figure 2: An Architectural Overview of a Target Flash Device with Gated Clock



through the flash bus and executes the buffer management layer and the flash translation layer. The buffer management layer manages the buffer cache in the storage device. In many flash devices, the buffer cache is usually used for write buffering because a write operation is much slower than a read operation. Thus, in this work, the buffer cache is used as a write buffer.

The FTL emulates the functionality of a normal block device, providing an interface between the upper layer and the flash chips. The FTL maintains a small internal buffer for use in internal operations such as garbage collection. The flash chip is divided into several blocks, each of which consists of multiple pages. It has on-chip registers that are used as temporary storage for data transfers between the FTL buffer and the flash chip. The size of an on-chip register is the same as that of a page. A set of pages that share the same on-chip register is called a plane and there are usually 2-4 planes in a chip. Writing a page from the buffer cache to the flash chip requires several data transfers. A page in the buffer cache is first moved to the internal buffer of the FTL through a system bus. Then, it is sent to the on-chip register of the flash chip via the flash bus. The page data is finally written to the target flash page.

The time taken to write a page from the buffer cache to the flash chip is (Tb þ Tt þ Tw), denoted by Tb!f , where Tb is the time to move a page between the FTL and the buffer cache, Tt is the time to transfer a page through the flash bus, and Tw is the time to write a page to the flash chip from the on-chip register. The time taken to read a page from the flash chip to the FTL is (Tr þ Tt), where Tr is the time to read a page from the flash chip to the on chip register. Note that if there is a host read request, data loaded into the FTL buffer is directly transferred to the host interface because the buffer cache is used as a write buffer Typical values of Tr, Tw, and Tt are 25, 200, and 100 _s, respectively. Tb is assumed tobe 0 because data is transferred using a high-speed system bus. A page migration also involves several data transfers. Suppose that the page pk in Figure 2 is moved to the page pnew k. The page pk is first moved to the on-chip register and then is sent to the FTL buffer.

To reduce the cost of a page migration, most flash chips employ a specialized page copy operation, called a copy-back operation. With a copy-back operation, the page pk loaded in the on-chip register is directly written to the destination page pnew k . Thus, the time taken for a page migration is reduced to (Tr þ Tw) because data transfers between the processor and the flash chip are eliminated. Note that a copy-back operation can be used only when both the source and destination pages belong to the same plane. For the FTL to be buffer-aware, it should be able to access the contents of a buffer cache. In ourtarget device, the buffer management layer and theflash translation layer run on the same system, so it iseasy to share information between two layers. Manyflash devices such as embedded flash devices andsolid-state drives satisfy our target architecture.

By eliminating useless page migrations, thebuffer-aware block merge performs a block mergeoperation at a lower cost than the buffer-unawareblock merge. To understand the effect of the bufferawareblock merge on performance, we first comparethe buffer-unaware block merge cost and the bufferawareblock merge cost. The buffer-unaware andbuffer-aware block merge cost. In the buffer-unawareblock merge, the block merge cost is determined bythe number of pages

that are moved between flashblocks during a block merge.

A synchronized enable condition allows theregister bank to receive either new data from D_IN,or recycled data, depending on the condition of theenable line. But in each of these conditions, the clockcontinues to toggle the register every time, whichdissipates dynamic power. When clock gating isadded, if the enable condition is not on, then theregister bank is not clocked, which saves power. Theclock-gating cell is an integrated clock-gating (ICG)cell. Compared with using discrete AND gates, ICGcells save power are more area-efficient and are lesslikely to cause clock-skew problems. To reduce thepower consumption in flash storage device.

SIMULATION RESULTS

By eliminating useless page migrations, thebuffer-aware block merge performs a block mergeoperation at a lower cost than the buffer-unawareblock merge. To identify the invalid pages andto delete the invalid pages from memory. Buffer Aware Garbage Collection using two algorithm buffer aware block merge and bufferaware victim block selection.

Figure 3: Simulation Result for Identify the Invalid Page in Memory

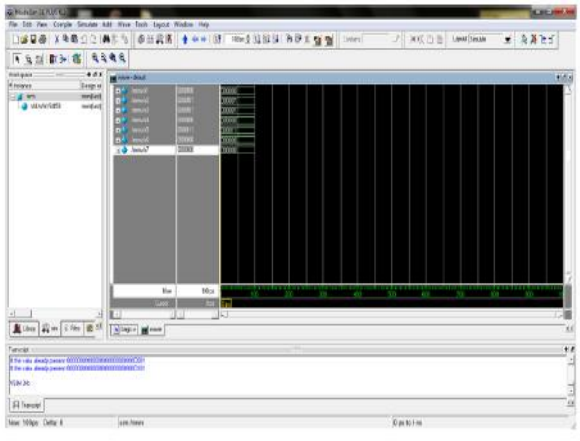
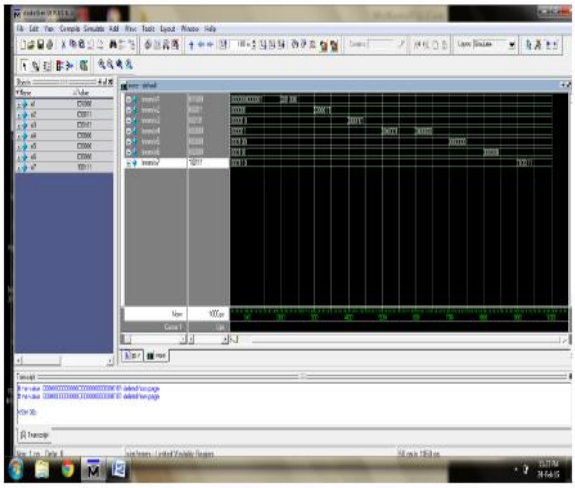


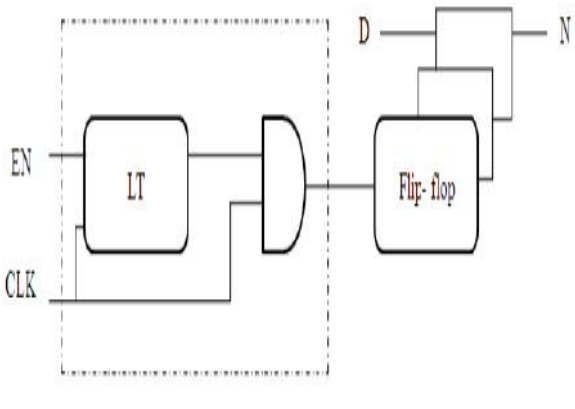
Figure 4: Simulation Result for Delete the Invalid Page in Memory



FURTHER IMPLEMENTATION

The gated clock method is used to implemented in flash storage device. Gated clock is amethod for reducing power consumption in memories.By this method the clock signal is not applied to theflip flop when the circuit is in idle condition.

Figure 5: Gated Clock Method



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gating(ICG) cell. Compared with using discrete AND gates,ICG cells save power are more area-efficient and areless likely to cause clock-skew problems

CONCLUSION

Experimental results show the to identify theinvalid pages and to delete the invalid page frommemory. The gated clock method is used toimplemented in flash storage devices. To reduce the power consumption.

REFERENCES

1. Wu M and Zwaen Poel W (1994), "eNVy: A Non-Volatile, Main Memory Storage System, Proc. Int'lConf", *Architectural Support for Programming Languages and Operating Systems*, pp. 86-97.
2. Kim H J and Lee S G (1999), "A New Flash MemoryManagement for Flash Storage System", *Proc. Computer Software and Applications Conf.*, pp. 284-289.
3. Li H L, Yang C L and Tseng H W (2008), "Energy-Aware Flash Memory Management in VirtualMemory System", *IEEE Trans. Very Large ScaleIntegration Systems*, Vol. 16, No. 8, pp. 952-964.
4. Ban A (1995), "Flash File System", US patent 5,404,485,Washing ton, DC, Patent and Trademark Office, April.
5. Kim J, Kim J M, Noh S H, Min S L and Cho Y (2002), "A Space- Efficient Flash Translation Layer forCompact Flash Systems", *IEEE Trans. Consumer Electronics*, Vol. 48, No. 2, pp. 366-375.
6. Lee S W, Park D J, Chung T S, Lee D H, Park S, and Song H J (2007), "A Log Buffer Based FlashTranslation Layer Using Fully Associative Sector Translation", *ACM Trans. Embedded Computing Systems*, Vol. 6, No. 3, pp. 1-27.
7. Kang J U, Jo H, Kim J S, and Lee J (2006), "ASuperblock-Based Flash Translation Layer for NAND Flash Memory", Proc. Int'l Conf. Embedded Software, pp. 161-170.
8. Ji S and Shin D (2010), "Locality and Duplication-Aware Garbage Collection for Flash Memory-BasedVirtual Memory Systems", *Proc. Int'l Conf.Computer and Information Technology*, pp. 1764-1771.
9. Boyd J (July 2008), "Mixing Memory To SpeedSolid-State Drives", *IEEE Spectrum*, (OnlineArticle).
10. Mearian L (June 18, 2009), "Review: Hard disk vs. solid-state drive — is an SSD worth themoney?", *Computer World*, (Online Article).

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